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FINAL REPORT

for

PLATED WIRE MEMORY SUBSYSTEM

May 1970 - May 1972

Contract No.: NAS5-20155

Prepared by

Motorola Inc.

Government Electronics Div.

Scottsdale, Arizona

for

Goddard Space Flight Center

Greenbelt, Maryland

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Contract No.: NAS5-20155

Goddard Space Flight Center

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1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola, Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS5-20155. The report is submitted in accordance with the requirements of Specifications S-562-P-24 and S-250-P-1A and covers the period from May 1970, to May 1972.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the design, development, construction and testing of a 4000 word by 18 bit random access, NDRO Plated Wire Memory for use in conjunction with a Spacecraft Input/Output Unit and Central Processing Unit.

The primary design parameters, in order of importance, were high reliability, low power, volume and weight. A single memory unit, referred to as a "Qualification Model," was delivered.

1.2 RESULTS ATTAINED

The memory unit was subjected to comprehensive functional and environmental testing at the end-item level to verify conformance with the specified requirements. Contract modifications were necessary in some areas, either to relax the requirements or to redefine noncritical parameters. All such modifications were relatively insignificant, with the possible exception of system weight and operating power consumption which, as exhibited by the delivered memory unit, were within the limits reflected in the original equipment specification (S-562-P-24) but would not meet the requirements as specified in Article XX of the contract schedule (6 pounds and 6 watts versus 4.5 pounds and 4 watts, respectively). The limits were revised to 5.5 pounds and 6 watts via subsequent contract modifications.

A comparison of the memory unit's most significant physical and performance characteristics versus the specified requirements is shown in Table I.

Table I. Memory Performance vs. Specified Requirements

Characteristic	Contract Reference	Specified	Measured
Volume	S-562-P-24 Mod. 3 (24 April 72)	125 in^3 127 in^3	126.25 in^3
Weight	S-562-P-24 Art. XX (13 May 70) Mod. 3	6 lbs 4.5 lbs 5.5 lbs	5.41 lbs
Power (Operate)	S-562-P-24 Art. XX Mod. 1 (11 June 71)	6 watts 4 watts 6 watts	5.29 watts
Power (Standby)	S-562-P-24 Mod. 3	100 milliwatts 150 milliwatts	149 milliwatts
Voltage Tolerance	S-562-P-24 Art. XX	±5% on +5V ±2% on other ±5% on all	±5% on all
Operating Rate	S-562-P-24	500 kHz	>500 kHz
Access Time	S-562-P-24 Art. XX	700 nanoseconds 400 nanoseconds	<400 nanoseconds
Operating Temp.	S-562-P-24	$-40^{\circ}C$ to $+85^{\circ}C$	Tested from $-40^{\circ}C$ to $+85^{\circ}C$
Operating Vacuum	S-562-P-24 Mod. 3	One Atm. to 10^{-6} mm Hg. One Atm. to 10^{-5} mm Hg. (Modified for test purposes)	Tested from one Atm. to 10^{-5} mm Hg.

Table I. Memory Performance vs. Specified Requirements (Contd)

Characteristic	Contract Reference	Specified	Measured
Operating Vibration	S-562-P-24	Sinusoidal: 5-25Hz, 0.5 in DA 25-110Hz, 15g Peak 110-2000Hz, 7.5g Peak Two Octaves/Minute Random: 15Hz, $0.01g^2$/Hz 15-70Hz, Linear Increase 70-100Hz, $0.31g^2$/Hz 100-400Hz. Linear Decrease 400-2000Hz, $0.02g^2$/Hz Two Min. /Axis	Tested at specified levels.
Operating Shock	S-562-P-24	Two Shock Pulses of 30g for 6 and 12 milliseconds in three directions.	Tested at specified levels.

SECTION 2

HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design, construction and test history, as relating to the hardware requirements of the contract, is summarized herein. The summarization is in chronological order from date of contract award to date of final delivery of the memory unit.

Historically, three distinct, major phases evolved in development of the final configuration; the initial design and construction and two phases of redesign.

2.1 INITIAL DESIGN AND CONSTRUCTION

The contractual agreement was consummated on 13 May 1970 and the design activity was started immediately. Significant negative aspects of this design were as follows:

1. Conventional diode-matrix configuration for word current switching. This approach requires active switching at both terminations of the word straps. Also, since the memory stack would otherwise tend to "float", creating severe noise problems because of capacitive coupling, this approach requires maintenance of stack charge levels on non-addressed word lines. The problems due to the capacitance become particularly severe if magnetic "keepers" are used to reduce effects of adjacent bit disturb. Although relatively inefficient with respect to memory cycle time, power usage, implementation complexity and noise control, the diode matrix configuration has been the approach generally used for word current switching in plated-wire memories.

2. Absence of keepers. The negative decision with respect to keepers was based primarily on past trade-off analysis of the affects of the added capacitance and adjacent bit disturb problems. The weight of the keeper material, although significant, was a secondary consideration.

3. Use of uncompensated digit drivers. Because of characteristics inherent in the plated-wire storage elements, the digit current transmitted through the wire during write operations should ideally exhibit a positive temperature coefficient if the operating temperature range requirements are significant. The digit current sources used in the initial design were not temperature compensated and, in fact, exhibited a slight negative coefficient.

4. Use of plated-wire manufactured to maximize output level. Based on effects of memory operational profiles considered, at the time, as imposing the most severe requirements, this particular wire was considered optimum.

5. Internal memory timing developed from an astable multivibrator and ring counter. This approach permitted adjustment of timing sequences in discrete, clock-period steps only and, although satisfactory in other respects, was somewhat costly in terms of system power because cycle time could not be optimized.

6. Independent strobe generation. There were several stages of logic between the output buffer storage register (clocked by the read strobe) and the last common point of reference between control of word current and generation of the strobe. Thus optimum placement of the strobe position relative to the plated-wire output was difficult to maintain and subject to significant error.

Construction of the initial design was completed in December, 1970. However, the memory stack did not meet the electrical requirements over temperature, exhibiting severe skew. After extensive analysis of the problem, the cause was concluded to be flux in the tunnel structures, introduced during the soldering operation. Attempts to chemically "flush-out" the tunnels were not wholly successful and the decision was made to build a new memory stack.

Fabrication and test of the new stack was completed in March, 1971. System level check-out was started shortly thereafter. The memory unit functioned properly at room temperature, however, difficulties were experienced at temperature and voltage extremes when performing adjacent-bit-disturb tests. The problems were partially a result of not being able to write properly because of the uncompensated digit drivers. Because of these problems, the contract delivery date was extended to permit design and fabrication of improved digit drivers. This effort was started in May, 1971.

In the interim, the assembled memory unit was loaned to GSFC for preliminary interface testing.

2.2 FIRST REDESIGN

The new digit driver design necessitated layout and fabrication of new printed circuit boards for two of the electronics subassemblies. The timing and control assembly was also completely rebuilt to permanently incorporate improvements in internal system timing previously "hay-wired" in. These changes provided improved temperature stability of critical timing signals, lower power consumption because of more optimized timing, and faster access time.

Tests performed at GSFC included interleaved read/write test patterns (i.e. successive read cycles on particular word lines with write operations on adjacent word lines during alternate cycle times). The effects of such test patterns, which proved to be relatively severe with respect to test patterns normally used, had not been fully appreciated. The capability for generating such patterns was subsequently designed into the system level tester used at Motorola.

Upon return of the memory unit to Motorola (and prior to installation of the new digit driver and timing and control assemblies) magnetic sheet keepers were installed on one side of each plated-wire carrier structure to evaluate their effects. Some improvement was observed, however, because of constraints imposed on application of the keepers at the existing state of assembly ("loose" keepering on only one side of each carrier structure) the results were relatively inconclusive.

The three new board assemblies were installed in October, 1971. The plated-wires identified as marginal during previous testing were also replaced.

During subsequent testing at the system level, numerous bit errors were observed under conditions of high temperature and interleaved read/write test patterns. The memory stack was removed from the unit for comprehensive evaluation on a sophisticated, computer controlled test set-up which had been recently installed. Tests proved that the existing stack would not be useable without extensive rework because of residual materials (i.e. mold release) left in the tunnels after removal of the forming wires.

Cleaning of the tunnels by chemical and/or mechanical methods was proven feasible but was not considered to be the most desirable approach for the following reasons:

1. Removal of all plated-wire would be required, with only marginal assurance of success after one rework cycle.

2. New processes and techniques for stack construction, avoiding the problems assooiated with residual materials, had been developed and proven on sample units.

3. A much improved word-drive implementation had been designed and tested through in-house efforts. The new design was a less complex implementation, generated much less noise and was more compatible with the use of keepers.

4. New techniques for generation of system timing had also been developed which, in conjunction with the new word drive implementation, offered the potential for significant reduction in power consumption and better performance margins.

Consequently, several options were presented with recommendations that the memory stack should again be rebuilt, using the new word drive implementation with full keepering. Incorporation of the new timing circuitry was also recommended. This was the option exercised.

2.3 FINAL DESIGN

Fabrication and assembly of the final configuration was conpleted in March 1972.

In addition to the changes discussed previously, plated-wire with significantly improved "creep" and "crawl" characteristics was used in the new stack. The improvement was gained at some sacrifice in output level. Because of its relative imperviousness to adjacent-bit-disturb phenomenon, the new wire exhibited vastly improved operating margins.

Extensive worst-case testing was performed at both the memory stack and system level with good results. The predicted reduction in power consumption was also substantially achieved. The only problems encountered during formal, system-level testing were mechanical in nature (i.e. failure during vibration). After rectification of the problems, testing was successfully completed. Final delivery of the memory unit to GSFC was completed on 8 May 1972.

SECTION 3

TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figure 1. It is identified as Motorola Part Number 01-P13666B001, Serial Number 001.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Number 15-P13658B, Rev. X2 (included as an insert at the back of this report) completely defines the end-item package in terms of size, mounting pattern, finish, etc. The weight of the delivered unit was 5.41 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 2, Memory System Electrical Interface).

1. 18 Input Data Lines (to memory)
2. 16 Input Address Lines (to memory)
3. 18 Output Data Lines (from memory)
4. 1 Initiate Line (to memory)
5. 1 Read/Write Select Line (to memory)
6. 1 Read Complete Line (from memory)
7. 2 Thermistor Sensor Lines (from memory)
8. 7 Lines for -6.9V (to memory - all lines common internally)
9. 5 Lines for +5.0V (to memory - all lines common internally)
10. 12 Lines for Power and Signal Return (all lines common internally)

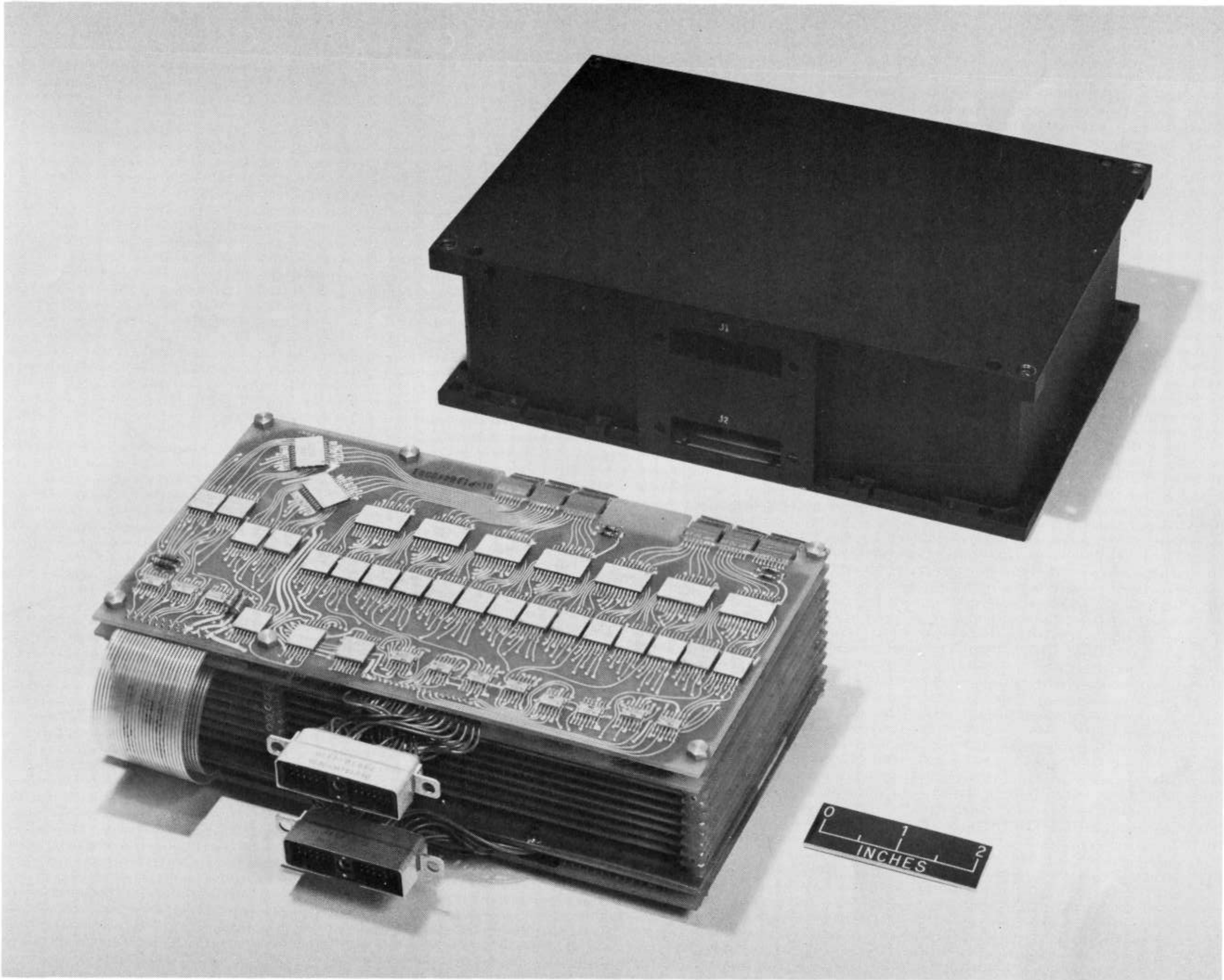

Figure 1. Low Power, Random Access Spacecraft Memory, Motorola Part Number 01-P13666B001.

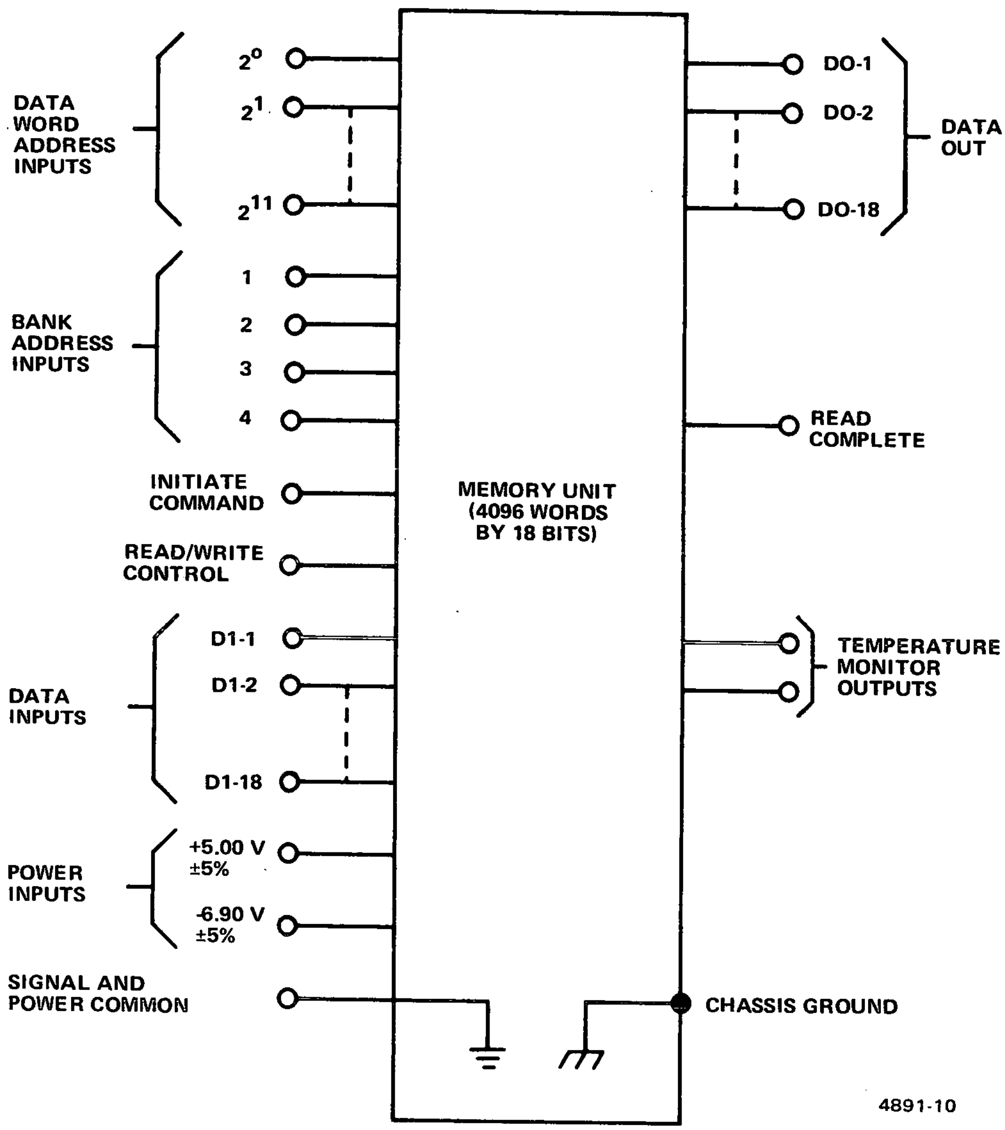

Figure 2. Memory System Electrical Interface

The connector pin designations are as given in Table II.

All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

<u>Memory Capacity:</u> 4096 words of 18 bits each (73,728 bits total).

<u>Access:</u> Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

<u>Access Time:</u> 350 nanoseconds, maximum, from leading edge of Initiate signal.

<u>Read Cycle Time:</u> 1.20 microseconds, maximum, from leading edge of Initiate signal.

<u>Write Cycle Time:</u> 1.00 microseconds, maximum, from leading edge of Initiate signal.

<u>Operate Rate:</u> 0 to 500k operations per second, minimum, with any read/write ratio.

<u>Initiate Signal:</u> Active level = logic ONE. Minimum pulse width = 50 nanoseconds. Maximum pulse width = 550 nanoseconds.

<u>Read/Write Select:</u> Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

<u>Bank Address Lines:</u> Must be at logic ONE level for minimum of 50 nanoseconds. Leading edge of Bank Address or Initiate (whichever occurs latest) defines start of cycle.

<u>Word Address Lines:</u> Must be stable from leading edge of Initiate to end of cycle time.

Table II. External Connector Pin Assignments

Pin No.	Function	Pin No.	Function
J1-1A	Address Bit 2^0	J2-1A	Data Input Bit 2^0
-1B	Address Bit 2^1	-1B	Data Input Bit 2^1
-1C	Address Bit 2^2	-1C	Data Input Bit 2^2
-1D	Address Bit 2^3	-1D	Data Input Bit 2^3
-1E	Address Bit 2^4	-1E	Data Input Bit 2^4
-1F	Address Bit 2^5	-1F	Data Input Bit 2^5
-1G	Address Bit 2^6	-1G	Data Input Bit 2^6
-1H	Return	-1H	Data Input Bit 2^7
-1J	Read/Write Control	-1J	Data Input Bit 2^8
-1K	Return	-1K	Data Input Bit 2^9
-1L	Return	-1L	Data Input Bit 2^{10}
-1M	Return	-1M	Data Input Bit 2^{11}
-1N	Initiate Command	-1N	Data Input Bit 2^{12}
-1P	Not Assigned	-1P	Data Input Bit 2^{13}
-2A	Address Bit 2^0	-2A	Data Input Bit 2^{14}
-2B	Address Bit 2^8	-2B	Data Input Bit 2^{15}
-2C	Address Bit 2^9	-2C	Data Input Bit 2^{16}
-2D	Address Bit 2^{10}	-2D	Data Input Bit 2^{17}
-2E	Address Bit 2^{11}	-2E	Data Output Bit 2^0
-2F	Bank Address Bit 0	-2F	Data Output Bit 2^1
-2G	Bank Address Bit 1	-2G	Data Output Bit 2^2
-2H	-6.9V	-2H	Data Output Bit 2^3
-2J	-6.9V	-2J	Data Output Bit 2^4
-2K	-6.9V	-2K	Data Output Bit 2^5
-2L	-6.9V	-2L	Data Output Bit 2^6
-2M	-6.9V	-2M	Data Output Bit 2^7
-2N	-6.9V	-2N	Data Output Bit 2^8

Table II. External Connector Pin Assignments (Contd)

Pin No.	Function	Pin No.	Function
J1-2P	-6.9V	J2-2P	Data Output Bit 2^9
-3A	Bank Address Bit 2	-3A	Data Output Bit 2^{10}
-3B	Bank Address Bit 3	-3B	Data Output Bit 2^{11}
-3C	+5.0V	-3C	Data Output Bit 2^{12}
-3D	+5.0V	-3D	Data Output Bit 2^{13}
-3E	+5.0V	-3E	Data Output Bit 2^{14}
-3F	+5.0V	-3F	Data Output Bit 2^{15}
-3G	+5.0V	-3G	Data Output Bit 2^{16}
-3H	Thermistor	-3H	Data Output Bit 2^{17}
-3J	Thermistor	-3J	Return
-3K	Read Complete	-3K	Return
-3L	Return	-3L	Return
-3M	Return	-3M	Return
-3N	Not Assigned	-3N	Return
-3P	Not Assigned	-3P	Return

Input Date Lines: For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

Read Complete Line: Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 350 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

Data Output Lines: Presents high impedance state (20k minimum) in quiescent state. Goes active (i.e. low impedance) maximum of 30 nanoseconds following leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. (Subsequent units would be designed to prohibit active level on Data Output lines from starting prior to active level on the Read Complete Line and to constrain maximum duration of active level on Data Output lines to 600 nanoseconds). Will sink minimum of 10 mA at 0.3 V in active state.

3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.9V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

<u>+5.0V:</u>

Regulation: ±5%

Average Standby Current: 21 mA, worst-case.

Average Operate Current: 665 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 50 mA, maximum, during cycle time.

Standby Power: 111 milliwatts maximum at +5.25V.

Operate Power: 3.50 watts, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

<u>-6.9V:</u>

Regulation: ±5%

Average Standby Current: 5.3 mA, worst-case.

Average Operate Current: 249 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 60 mA, maximum, during cycle time.

Standby Power: 38.5 milliwatts, maximum, at -7.25 volts.

Operate Power: 1.81 watts, maximum, at -7.25 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table III.

Table III. Thermistor Resistance Versus Temperature

RESISTANCE VERSUS TEMPERATURE −80°C to +150°C

TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES
−80	3558K	−50	441.3K	−20	78.91K	+10	18.79K	+40	5592	+70	1990	+100	816.8	+130	376.4
79	3296K	49	414.5K	19	74.91K	11	17.98K	41	5389	71	1928	101	794.6	131	367.4
78	3055K	48	389.4K	18	71.13K	12	17.22K	42	5193	72	1868	102	773.1	132	358.7
77	2833K	47	366.0K	17	67.57K	13	16.49K	43	5006	73	1810	103	752.3	133	350.3
76	2629K	46	344.1K	16	64.20K	14	15.79K	44	4827	74	1754	104	732.1	134	342.0
75	2440K	45	323.7K	15	61.02K	15	15.13K	45	4655	75	1700	105	712.6	135	334.0
74	2266K	44	304.6K	14	58.01K	16	14.50K	46	4489	76	1648	106	693.6	136	326.3
73	2106K	43	286.7K	13	55.17K	17	13.90K	47	4331	77	1598	107	675.3	137	318.7
72	1957K	42	270.0K	12	52.48K	18	13.33K	48	4179	78	1549	108	657.5	138	311.3
71	1821K	41	254.4K	11	49.94K	19	12.79K	49	4033	79	1503	109	640.3	139	304.2
−70	1694K	−40	239.8K	−10	47.54K	+20	12.26K	+50	3893	+80	1458	+110	623.5	+140	297.2
69	1577K	39	226.0K	9	45.27K	21	11.77K	51	3758	81	1414	111	607.3	141	290.4
68	1469K	38	213.2K	8	43.11K	22	11.29K	52	3629	82	1372	112	591.6	142	283.8
67	1369K	37	201.1K	7	41.07K	23	10.84K	53	3504	83	1332	113	576.4	143	277.4
66	1276K	36	189.8K	6	39.14K	24	10.41K	54	3385	84	1293	114	561.6	144	271.2
65	1190K	35	179.2K	5	37.31K	25	10.00K	55	3270	85	1255	115	547.3	145	265.1
64	1111K	34	169.3K	4	35.57K	26	9605	56	3160	86	1218	116	533.4	146	259.2
63	1037K	33	160.0K	3	33.93K	27	9227	57	3054	87	1183	117	519.9	147	253.4
62	968.4K	32	151.2K	2	32.37K	28	8867	58	2952	88	1149	118	506.8	148	247.8
61	904.9K	31	143.0K	− 1	30.89K	29	8523	59	2854	89	1116	119	494.1	149	242.3
−60	845.9K	−30	135.2K	0	29.49K	+30	8194	+60	2760	+90	1084	+120	481.8	+150	237.0
59	791.1K	29	127.9K	+ 1	28.15K	31	7880	61	2669	91	1053	121	469.8		
58	740.2K	28	121.1K	2	26.89K	32	7579	62	2582	92	1023	122	458.2		
57	692.8K	27	114.6K	3	25.69K	33	7291	63	2497	93	994.2	123	446.9		
56	648.8K	26	108.6K	4	24.55K	34	7016	64	2417	94	966.3	124	435.9		
55	607.8K	25	102.9K	5	23.46K	35	6752	65	2339	95	939.3	125	425.3		
54	569.6K	24	97.49K	6	22.43K	36	6500	66	2264	96	913.2	126	414.9		
53	534.1K	23	92.43K	7	21.45K	37	6258	67	2191	97	887.9	127	404.9		
52	501.0K	22	87.66K	8	20.52K	38	6026	68	2122	98	863.4	128	395.1		
51	470.1K	21	83.16K	9	19.63K	+39	5805	69	2055	99	839.7	129	385.6		

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3.3 FUNCTIONAL CHARACTERISTICS

An overall functional block diagram, data storage and word/digit electronics diagram and simplified memory drive and sense diagram for the diode matrix implementation (i.e. initial design) are shown in Figures 3 through 5. Corresponding diagrams for the transistor per word line implementation (i.e. final design) are shown in Figures 6 through 8.

3.3.1 Memory Organization

With respect to internal organization, both designs are identical. The memory is organized into 1024 memory words of 72 bits each. Each memory word therefore comprises four 18-bit external data words.

The internal organization evolved from the packaging approach. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

Using two wires for each bit storage (i.e. two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

In either design, the only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics was packaged as four two-sided printed circuit board assemblies in the diode-matrix implementation and as three similar board assemblies in the final (i.e. transistor-per-word line) implementation.

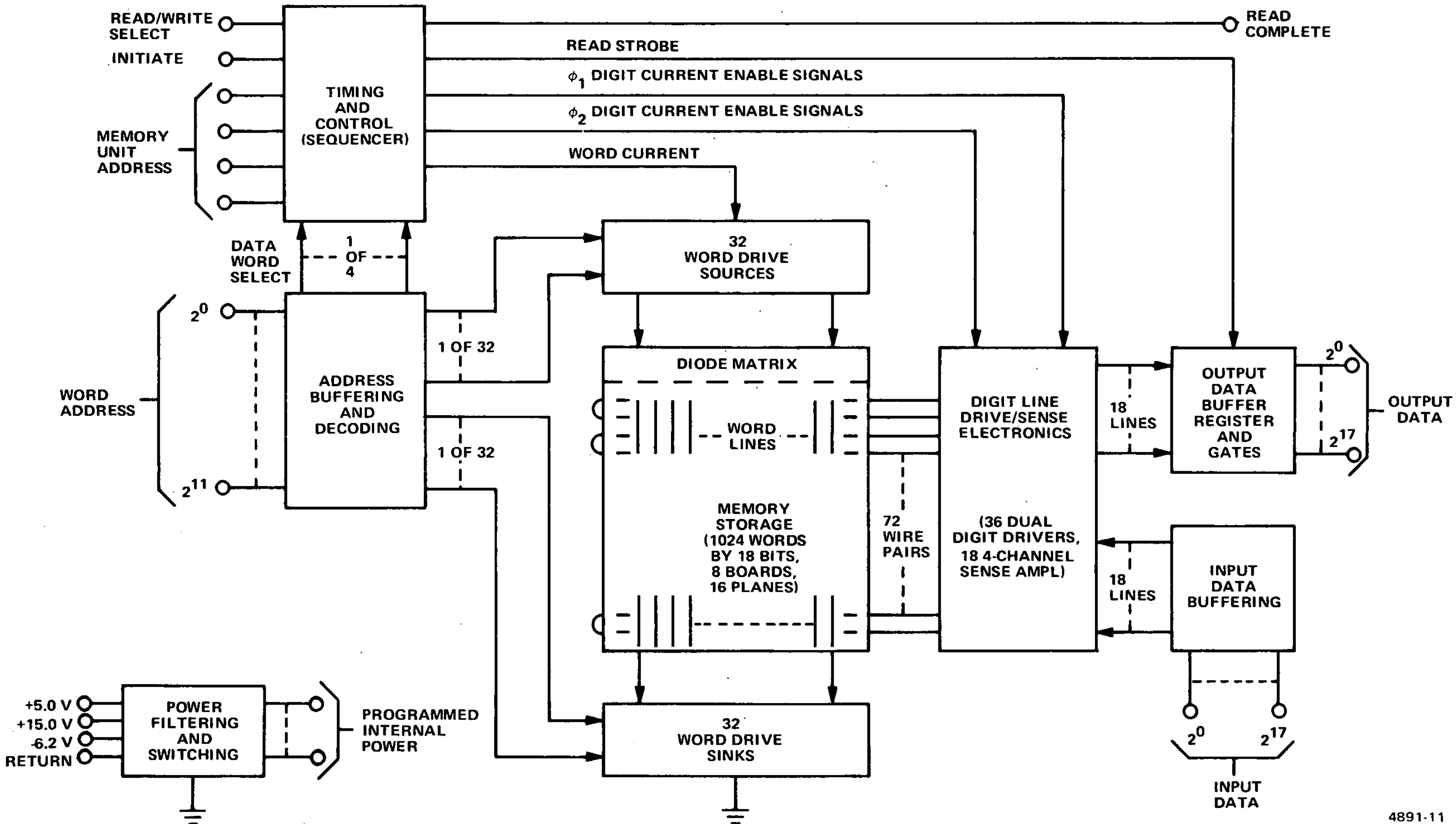


Figure 3. Overall Functional Block Diagram, Initial Design

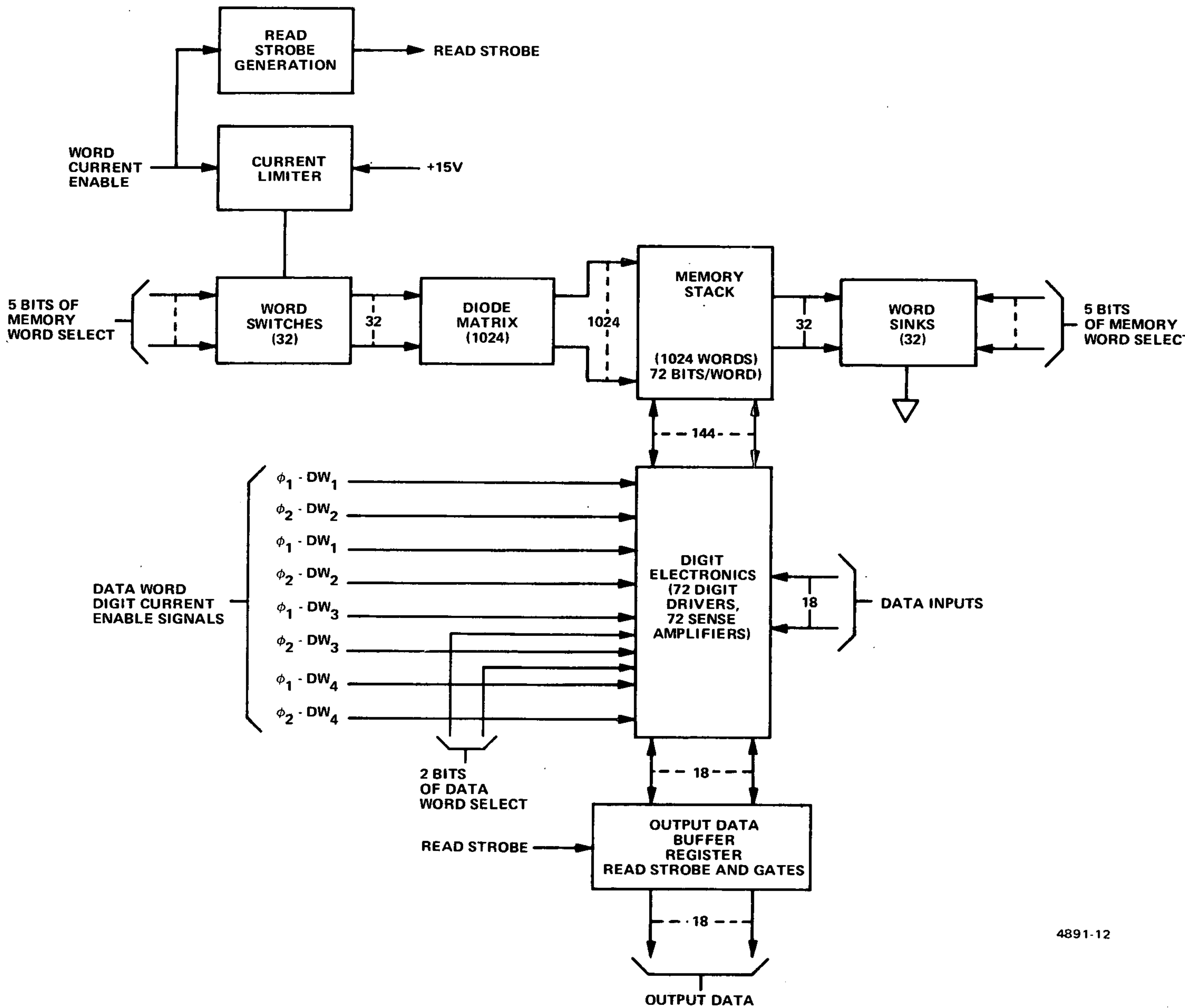


Figure 4. Data Storage and Word/Digit Electronics, Block Diagram, Diode Matrix Implementation

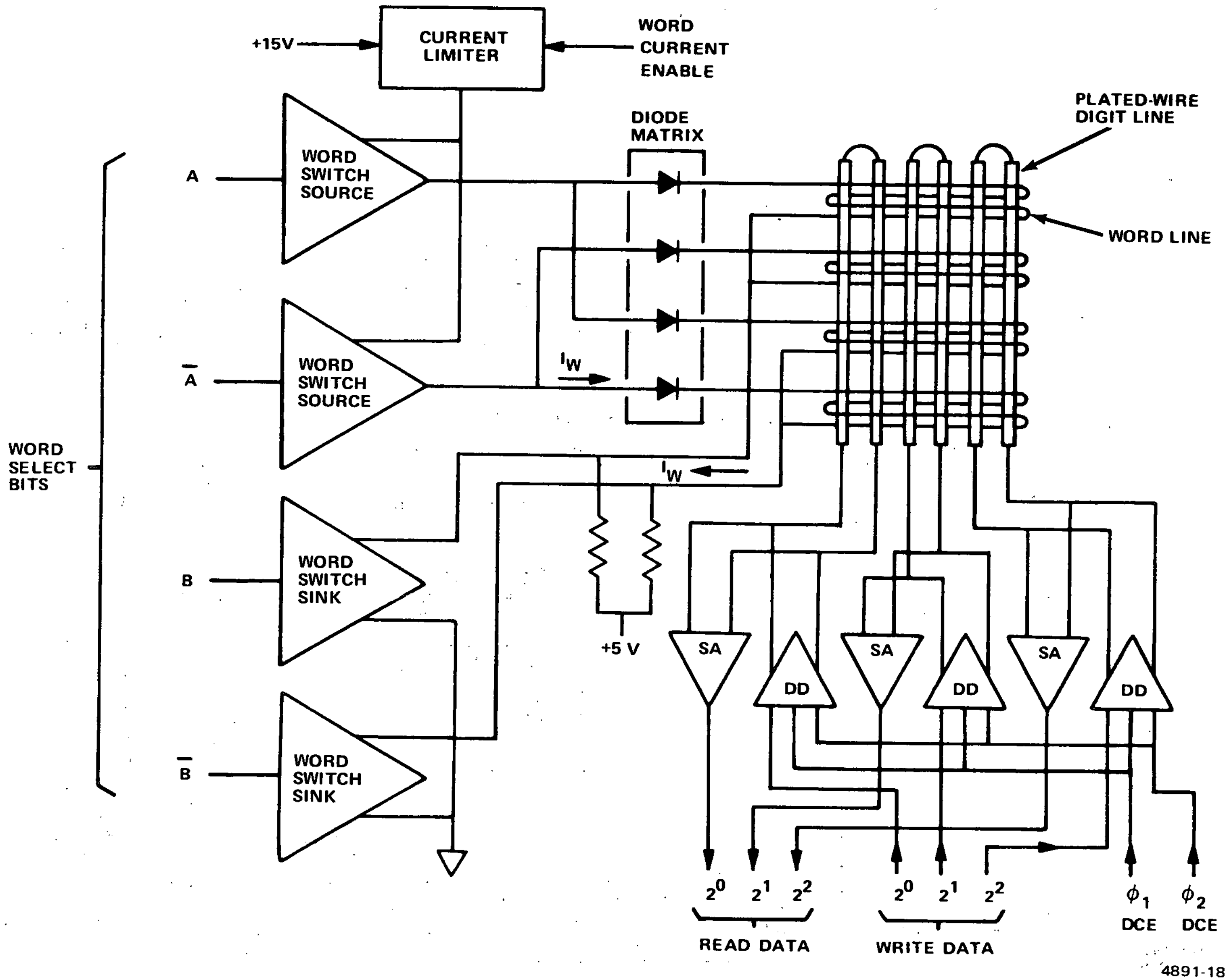


Figure 5. Simplified Memory Drive and Sense Diagram, Diode Matrix Implementation

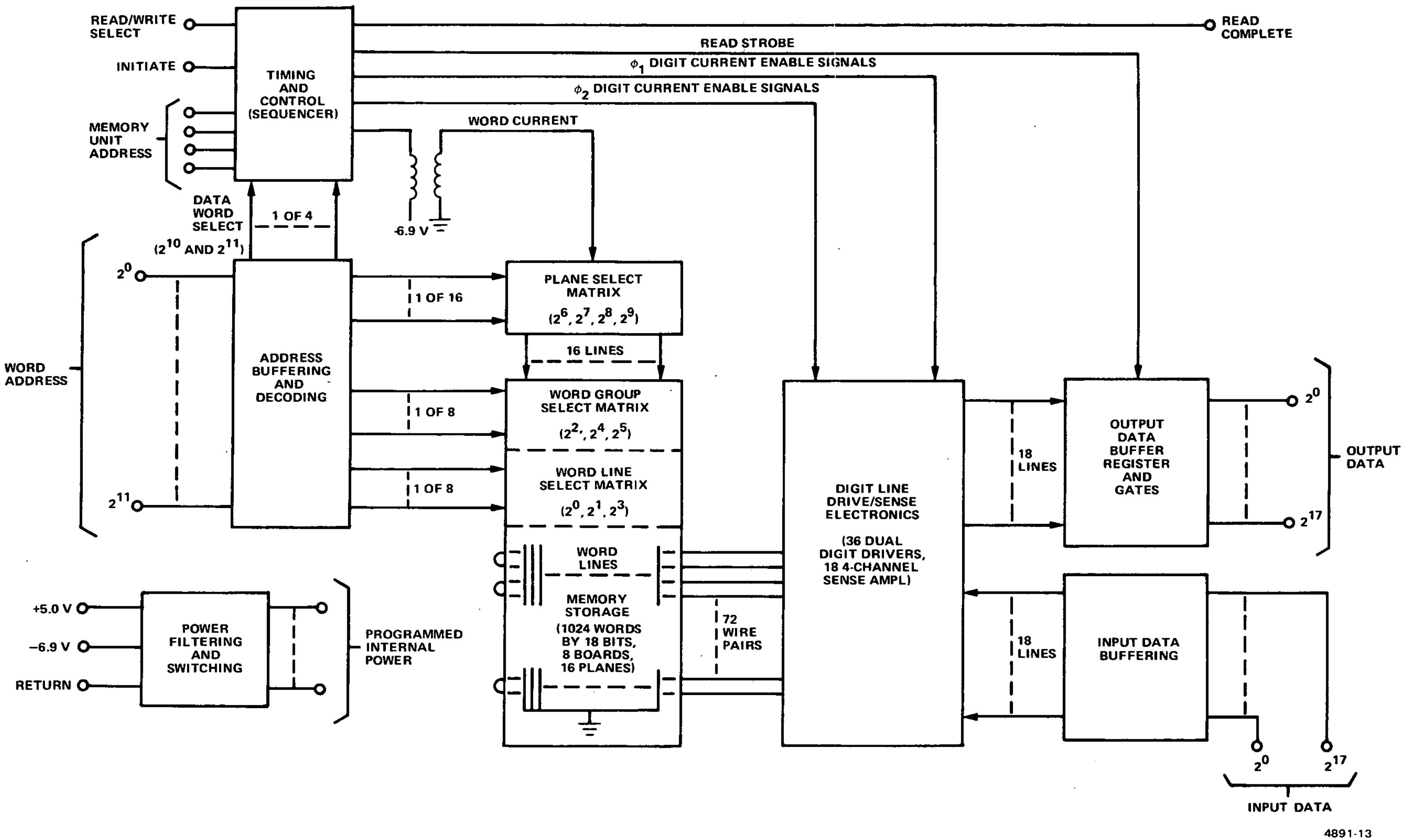


Figure 6. Overall Functional Block Diagram, Final Design

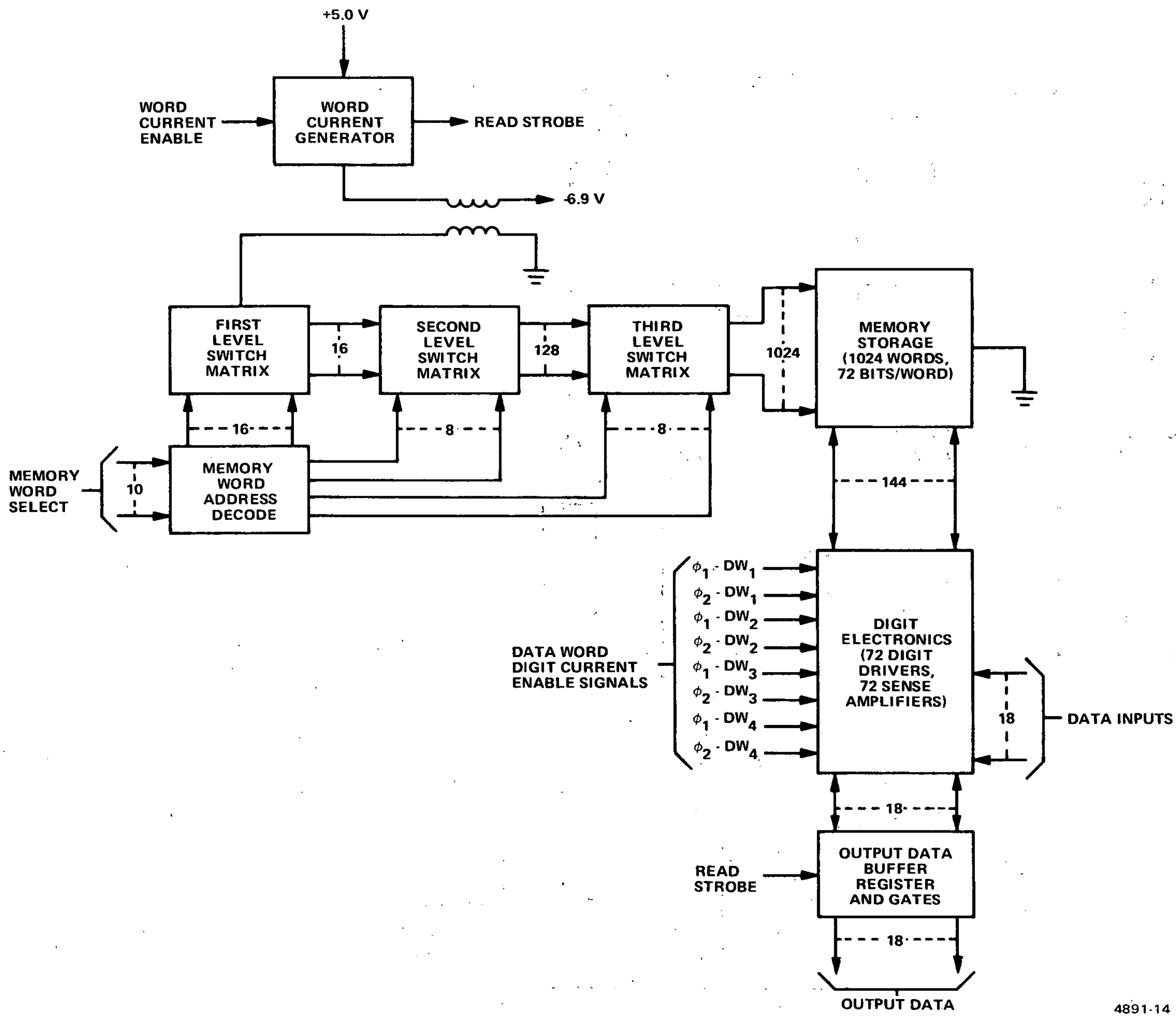


Figure 7. Data Storage and Word/Digit Electronics, Block Diagram, Transistor Switch Implementation

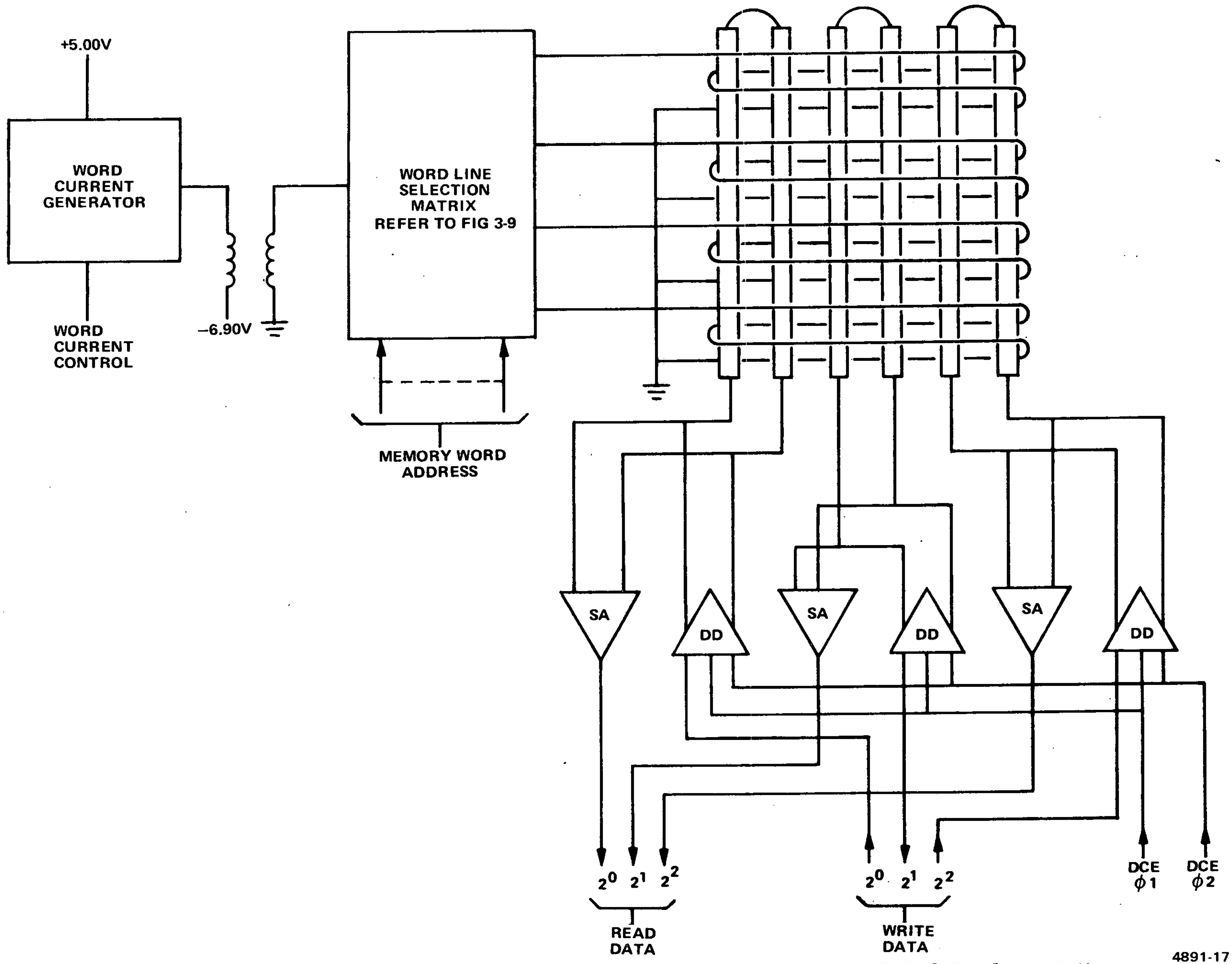


Figure 8. Simplified Memory Drive and Sense Diagram, Transistor Switch Implementation

3.3.2 Word-Line Selection and Drive

In the diode-matrix design, word-line selection was accomplished by actively switching both ends of the addressed word line. Implementation required a matrix of 32 word switch sources, 32 word switch sinks and 1024 isolating diodes. Each switch source was connected, through diodes, to 32 word lines. Each switch sink was connected to the opposite end of one word line from each switch source. Since each non-addressed word line must present a high impedance to the energized switch source, it was necessary to maintain (from a steady-state source) the charge level on stray capacitance associated with source activated/non-addressed word lines at a high enough level to prevent forward-biasing of the isolating diodes.

The diode-matrix implementation was relatively complex, quite noisy and slow because of charge transfer and stabilization requirements imposed by the stray capacitance.

Figures 8 and 9, together, show the word current selection and drive methods used in the final design.

Word line addressing is accomplished through a three-level tree of transistor switches. The first level steers the word current to one of 16 unique areas of the stack. One side of a memory stack board (i.e. a plane) comprises one of the sixteen unique areas. The first (or plane select) level is located in the sequencer. The second level further steers the word current to one of 8 word groups on the plane addressed via the first level. The third level finally steers the word current into one of 8 word lines in the particular word group addressed through the first two levels. The second and third levels are packaged on the memory stack boards.

The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits 2^6 through 2^9 are decoded into 1-of-16 and identify the plane. Bits 2^0, 2^1, and 2^3 are decoded into 1-of-8 and identify the word group. Bits 2^2, 2^4, and 2^5 are also decoded into 1-of-8 and identify the word line within the word group. Bits 2^{10} and 2^{11} identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight 1, 2, 4, 8, 16 - - - binary code.

Since only one end of each word line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from

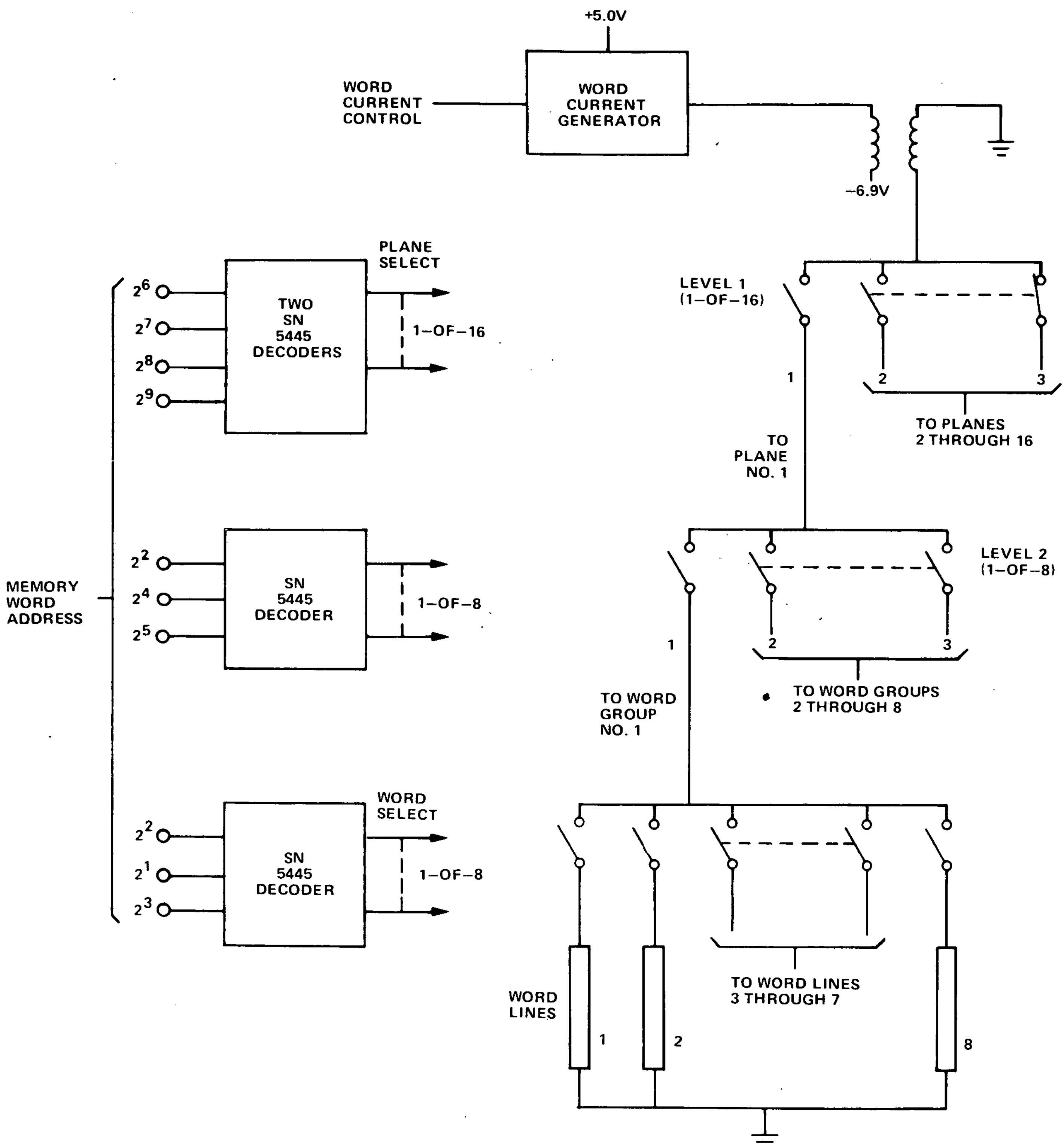


Figure 9. Word-Line Selection Matrix

charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing

Memory timing and control in the initial design was derived from a four-stage ring counter clocked by an astable multivibrator running at approximately 15 MHz. This is a very conventional approach but, where power consumption is a prime consideration and switching is used to minimize the average power required, not particularly efficient. The resolution at 15 MHz is only about 65 nanoseconds and events in the memory sequence could only be changed by this amount.

The final memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 10. Each dealy is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay τ_A (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers and associated logic is also controlled through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays τ_B through τ_E are activated for a write cycle. Delays τ_B and τ_D set the width of the two phases of digit current and τ_C sets the separation between the two phases. Delay τ_E controls the duration of the word current. The ϕ_1 and ϕ_2 digit current controls for one of the four possible data words are activated, depending on the states of address bits 2^{10} and 2^{11}.

Delays τ_F through τ_I are activated during a read cycle. Delay τ_F starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by τ_G and used as the read strobe, which

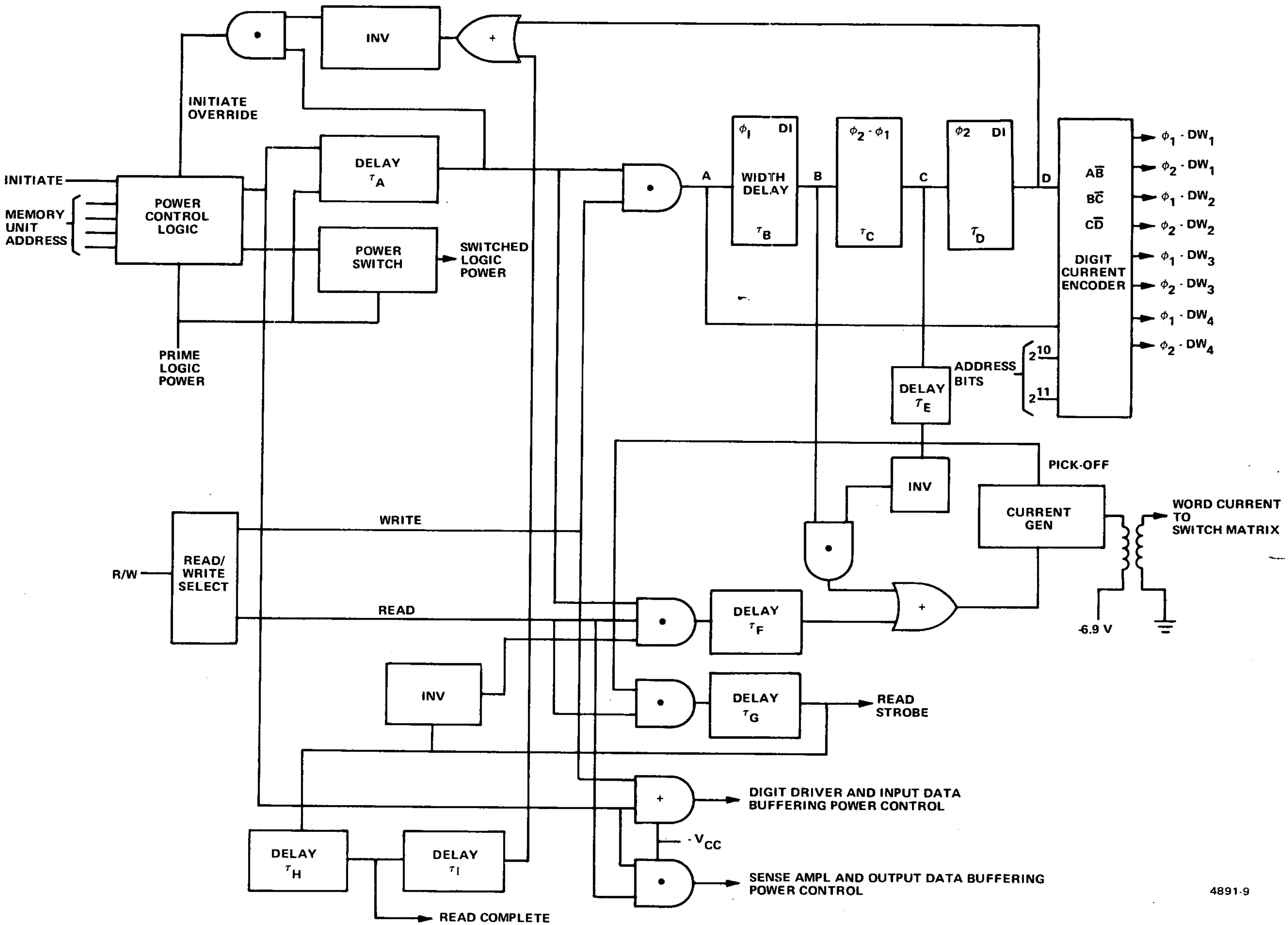


Figure 10. Sequencer, Logic Diagram

clocks the sense amplifier outputs into the output data buffer register. Delays τ_H and τ_I set the duration of the read complete and the post-read data hold periods, respectively.

3.3.4 Write Operation

The memory timing for a write cycle is shown in Figure 11. For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits 2^0 through 2^9. A group of 18 digit driver current sources is then energized for ϕ_1 current. The particular current sources are identified by address bits 2^{10} and 2^{11}. The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The ϕ_1 digit current is then terminated and ϕ_2 current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

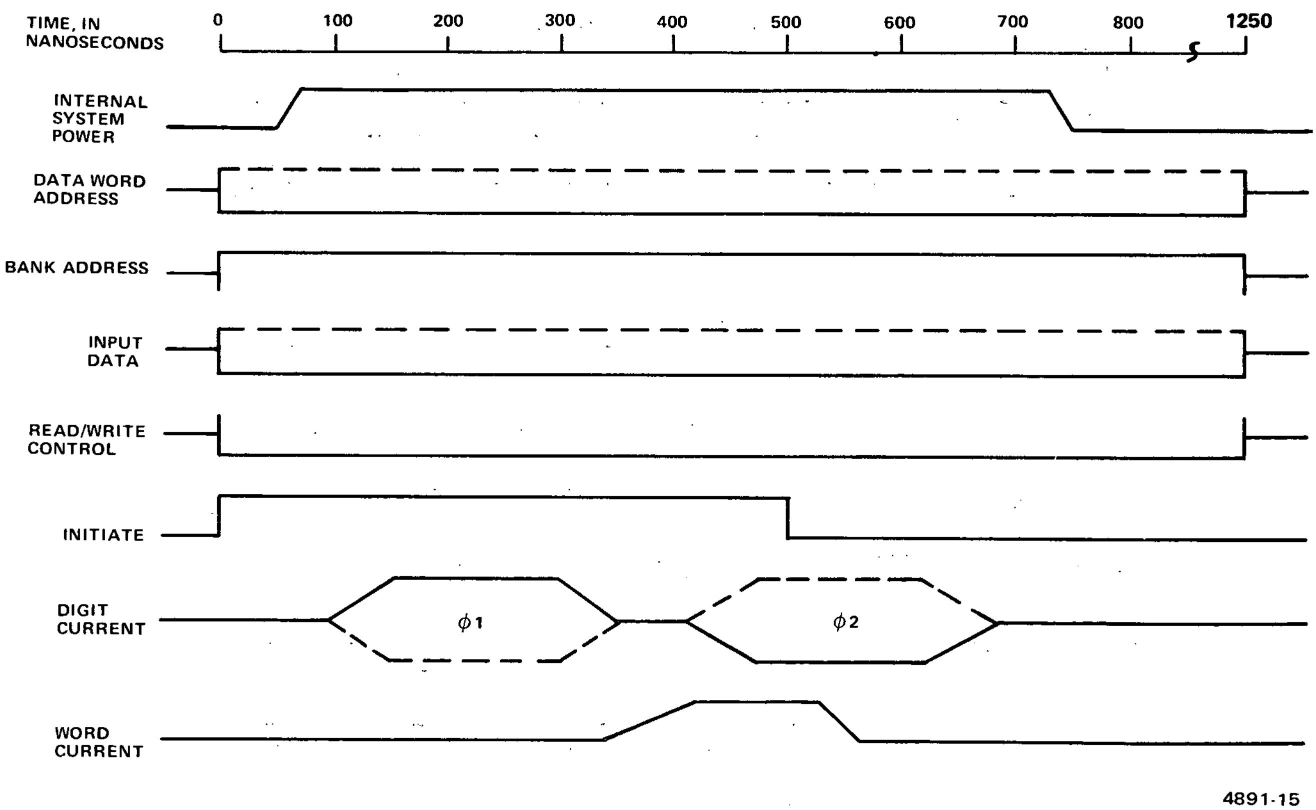


Figure 11. System Timing, Write Operation

The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when ϕ_2 digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the ϕ_2 digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in Figure 12. For proper operation, the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits 2^{10} and 2^{11}.

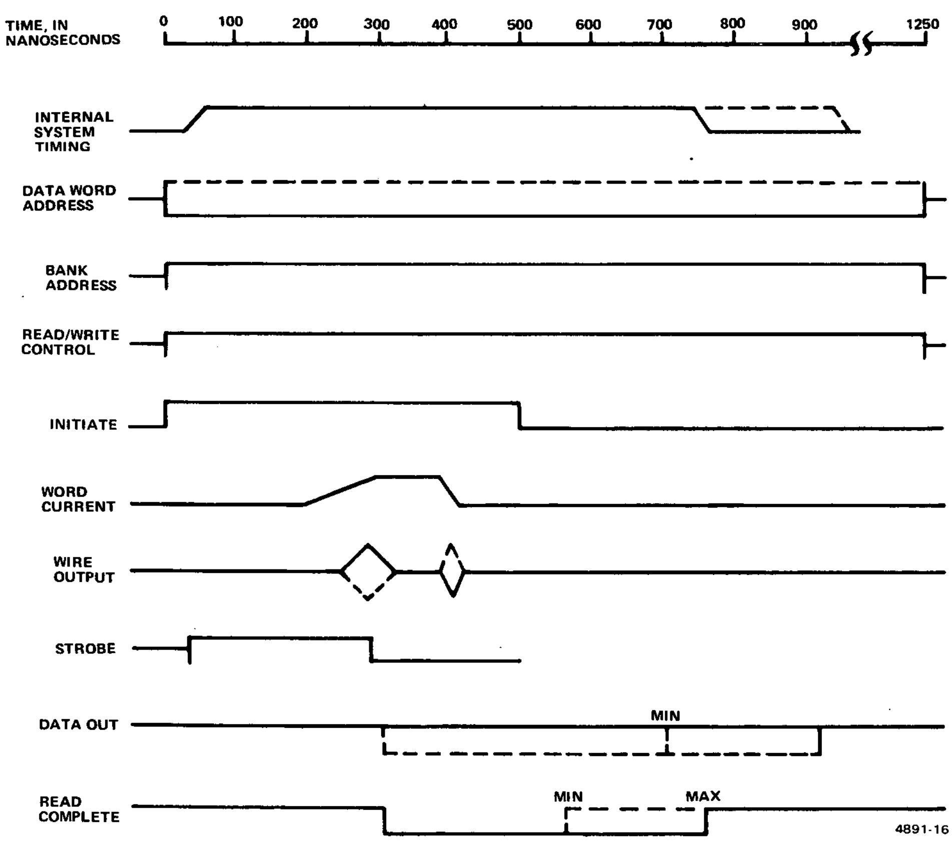


Figure 12. System Timing, Read Operation

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously "written into" the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is clocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e. output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out (per Figure 12) of a bit 0.

3.3.6 Power Requirements

The average power consumption in the memory is minimized through the use of solid-state power switches. During idle periods, power is switched off to all electronics except that required for detection of initiate commands and sequencer normalization. The nominal and worst-case maximum standby and operate power for operating rates of 500 kHz and read/write ratios of 1-to-1 and 4-to-1 are summarized in Table IV. As shown in the table the power is well within the specified 6 watts. Capacitive filtering is used on all power inputs to minimize the peak energy demands on the power source. Only two voltage inputs are required; +5.0 volts ±5% and -6.9 volts ±5%.

Table IV. Memory Power Requirements

	Nominal				Worst-Case			
	+5.00 V, +25°C		-6.90 V, +25°C		+5.25V, +85°C		-7.25 V, +85°C	
Standby Power	82.0 mW		12.5 mW		99.8 mW		30.5 mW	
Operate Power	4-1 R/W	1-1 R/W	4-1 R/W	1-1 R/W	4-1 R/W	1-1 R/W	4-1 R/W	1-1 R/W
	2.41 W	2.70 W	0.75 W	0.99 W	3.35 W	3.49 W	1.42 W	1.81 W
Maximum worst-case power = 4.76 W @4-1 R/W = 5.30 W @1-1 R/W								

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory.

3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. When available, these were procured per the requirements of Marshall Space Flight Center Specification 85M02716. Devices not available per this specification were procured per MIL-STD-883, Class B.

3.4.2 Discrete Resistors

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. Both types were procured to S failure-rate levels.

3.4.3 Discrete Capacitors

Three types of capacitors were used; the CSR13 style, established reliability tantalum with failure rate of R or lower, the CKR05 and 06 style, established reliability ceramic with failure rate of R or lower, and the CM series mica per MIL-C-5/18 with additional screening for DWV and IR.

3.4.4 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102, Condition C, except 10 cycles at -55^{o}C.

3.4.5 Discrete Transistors and Diodes

Only JANTX transistors and diodes were used in construction of the memory.

3.4.6 Hybrid Circuits

Eight different hybrid integrated circuits were used in the memory. These were all manufactured in-house and screened to requirements meeting or exceeding MIL-STD-883, Class B. (Operational vibration and power aging were waived on four of the eight types used in the final design). Each hybrid is briefly described, functionally, in the following paragraphs.

3.4.6.1 Delay Circuit

The delay circuit is shown, functionally, in Figure 13. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.6.2 Word Current Generator

The word current generator is shown in Figure 14. It consists, basically, of a controlled current source for which the turn-on slope and the amplitude are programmable by selection of external, discrete components. The current is gated on and off by an external enable signal. Input voltages are monitored and the word current is inhibited if voltage(s) is below a level of which the memory will operate properly.

There is also a level detector on the current output from which a trigger is developed for sampling the sense amplifier outputs during a read operation.

3.4.6.3 Word-Line Selection Circuits

The word line selection circuits are shown in Figures 15 and 16. A particular switch is closed by grounding the corresponding selection input. The first-level selection circuit is straightforward, a single input with four parallel, independently controlled switches to four outputs.

The second and third level switches are packaged together. A particular package contains one second level switch and two banks of four third level switches each. Each of four third level selection inputs controls one switch in each bank. A single selection input controls the second level switch. The pin-outs are configured so that a second level switch can be connected to a third level bank in a different package, as well as to a bank in its own package.

3.4.6.4 Sense Amplifier

The four-channel sense amplifier is shown in Figure 17. It consists of a monolithic MC 1546L amplifier clip in a special package with the input terminating resistors.

3.4.6.5 Digit Driver

The digit driver is shown in Figure 18. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The T1 and T2 inputs denote successive time periods for the two opposite phases of digit

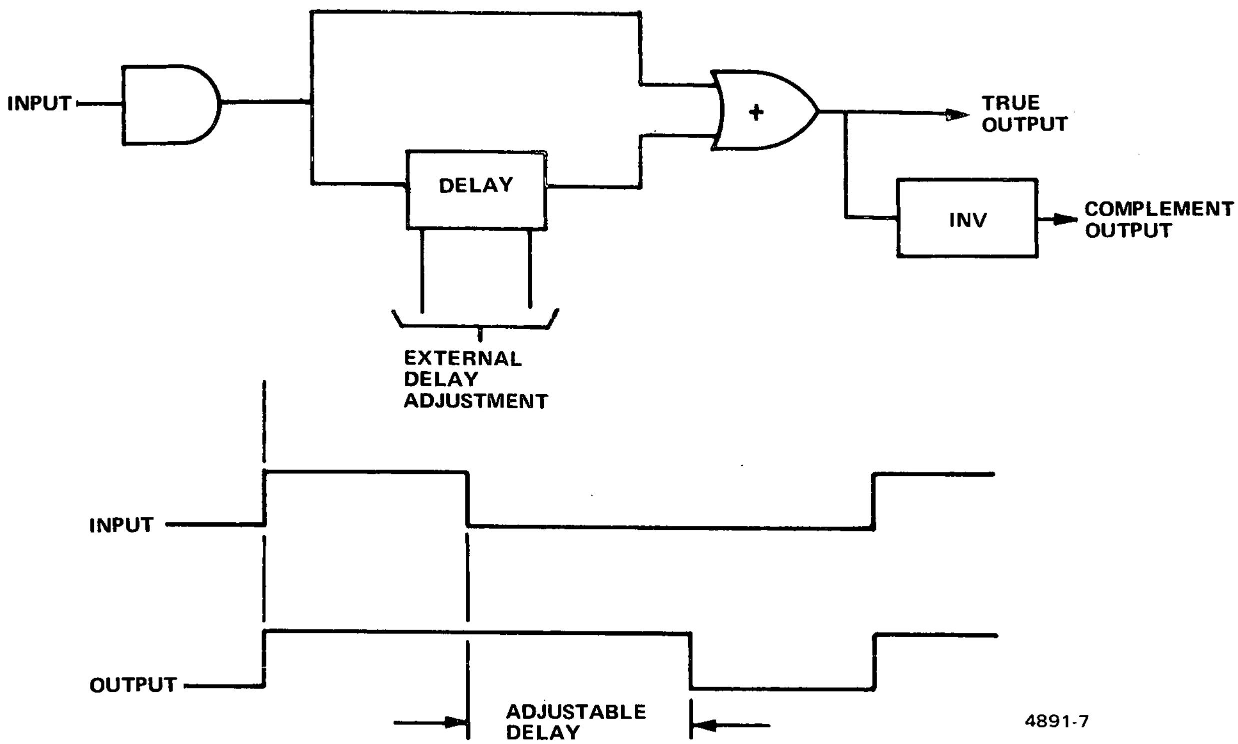


Figure 13. Delay Circuit, Functional Diagram

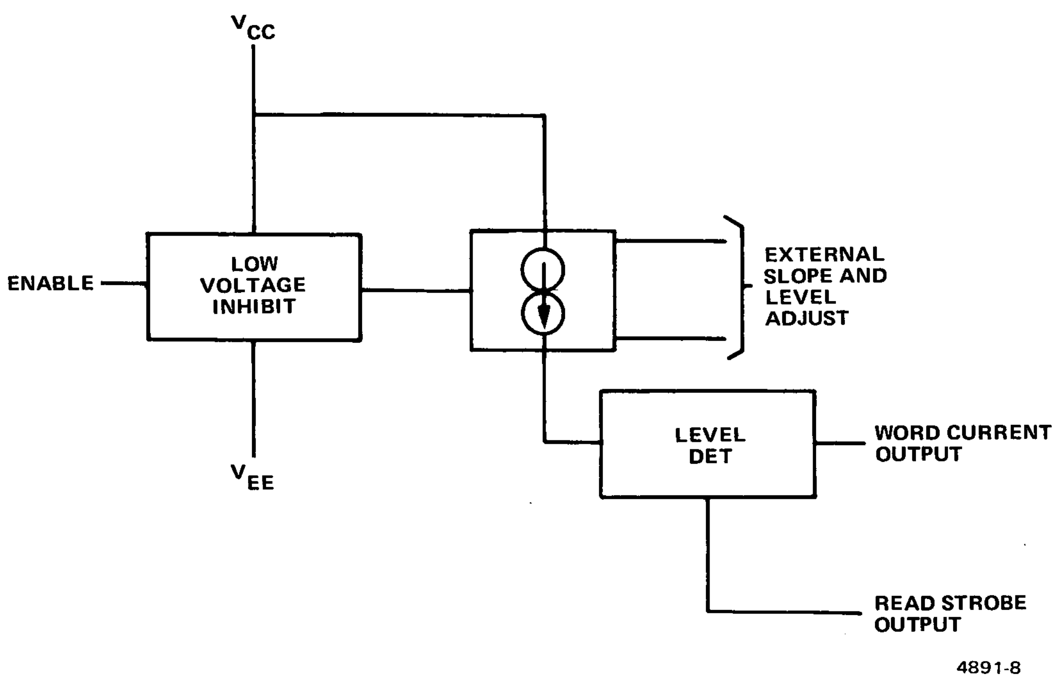


Figure 14. Word Current Generator, Functional Diagram

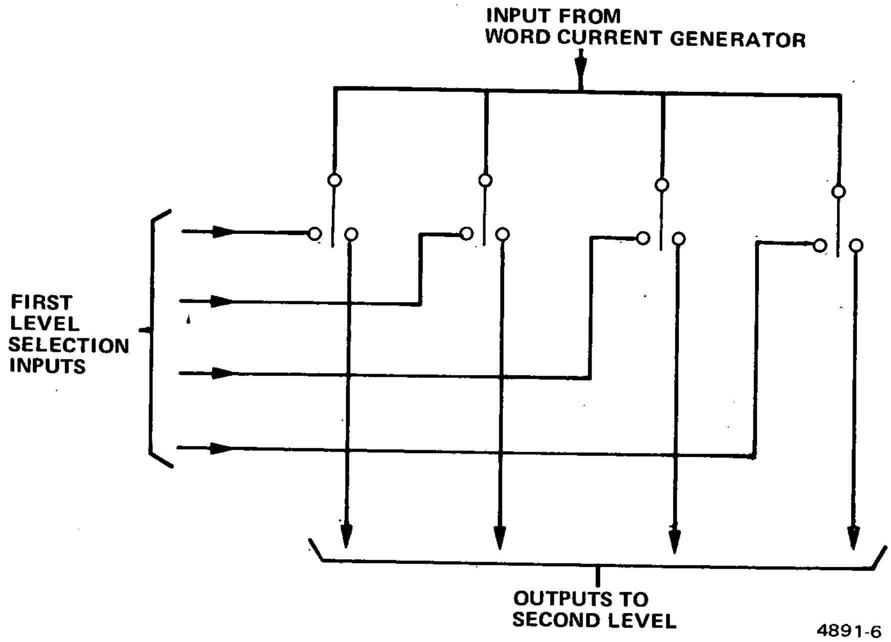


Figure 15. First Level Word-Line Selection Matrix, Functional Diagram

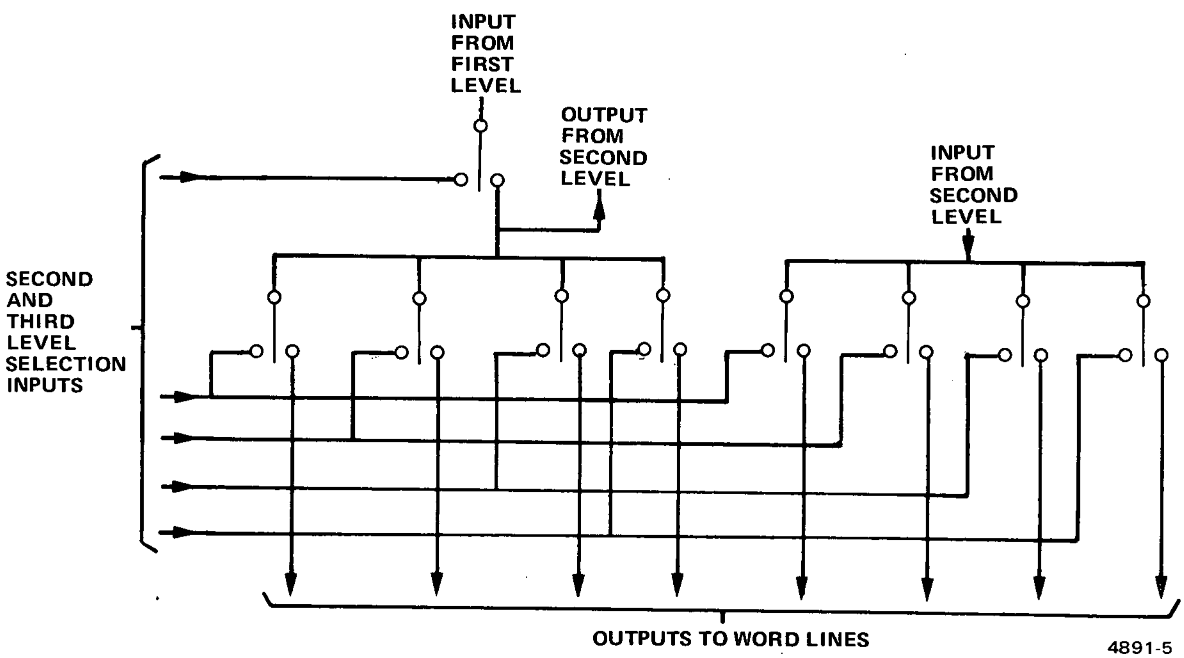


Figure 16. Second and Third Level Word-Line Selection Matrix, Functional Diagram

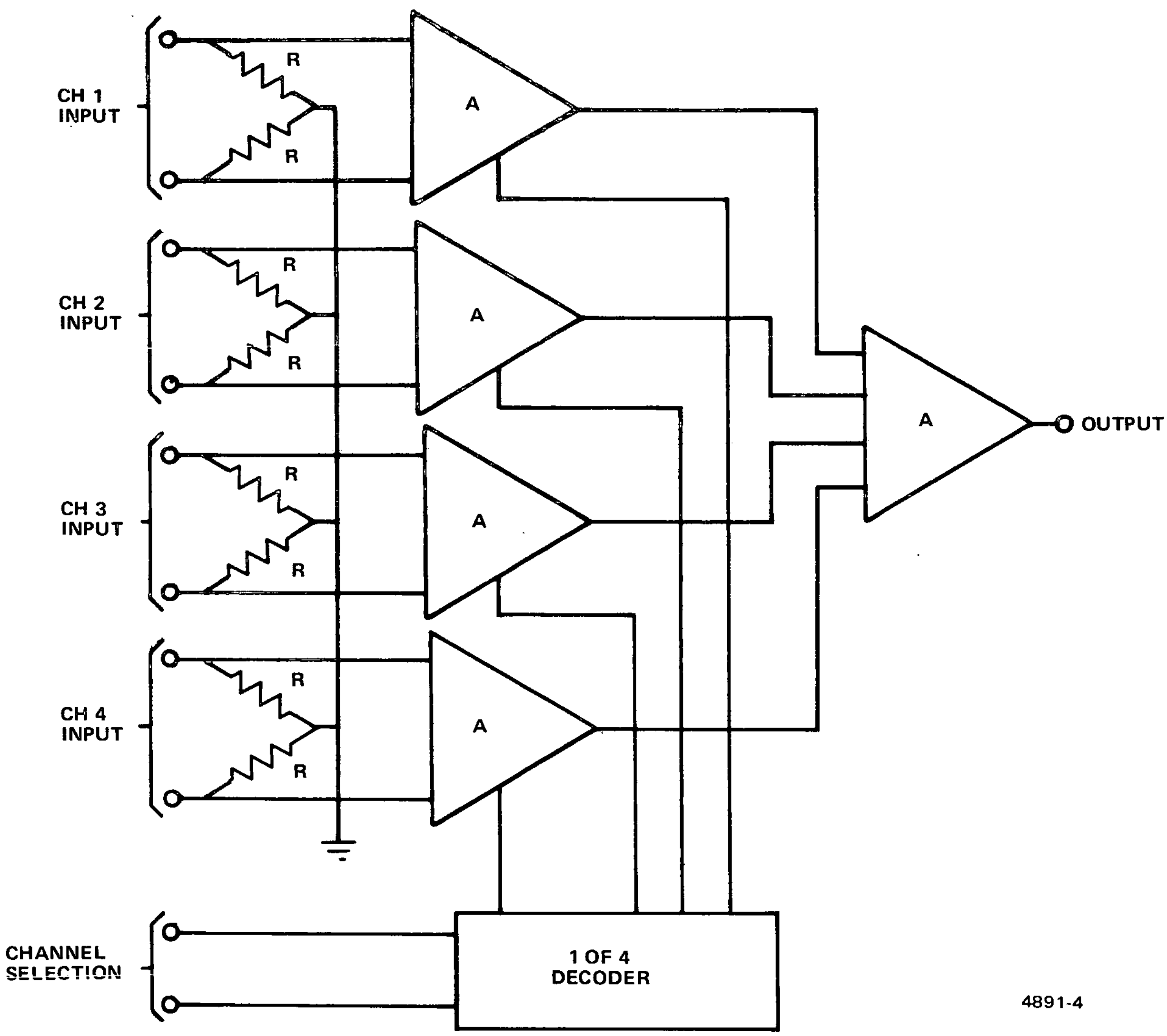


Figure 17. Four-Channel Sense Amplifier, Functional Diagram

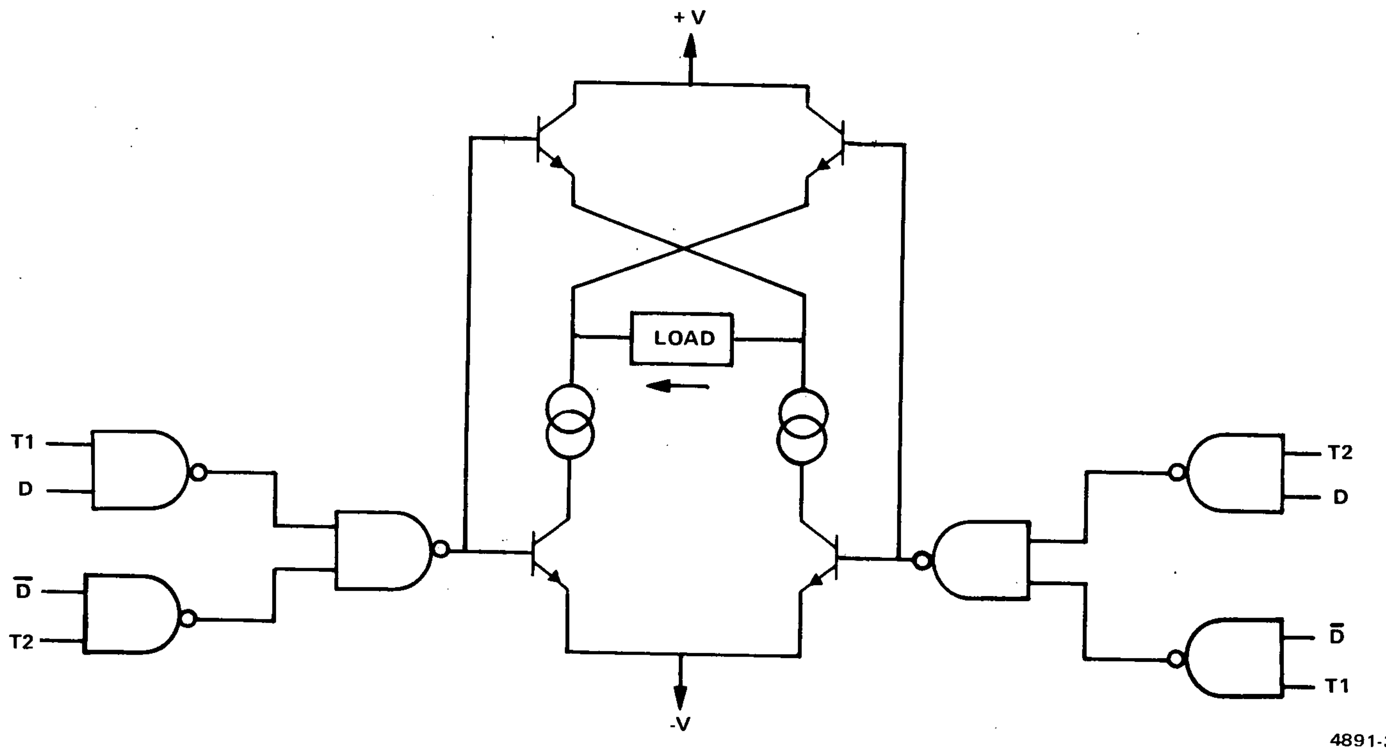


Figure 18. Digit Driver, Functional Diagram

current. The D and $\overline{D}$ inputs denote the true and complement levels of an input data bit. If D is true, then current will flow in the direction indicated during T1 and in the opposite direction during T2. The current flow would be opposite if $\overline{D}$ were true.

3.4.6.6 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.9 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 19 and 20.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.

3.5.1.1 Carrier Structure

The carrier structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polyimide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on polyimide film are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. The word lines are printed and etched on a single piece of film which is wrapped around one end of the tunnel matt to encircle the wire. A lap solder joint at the other end of the tunnel matt creates the double turn in the word line. Farther away from the matt, on the same end, is a "window" in the polyimide film where the conductors are unsupported and can be lap soldered to the mother board.

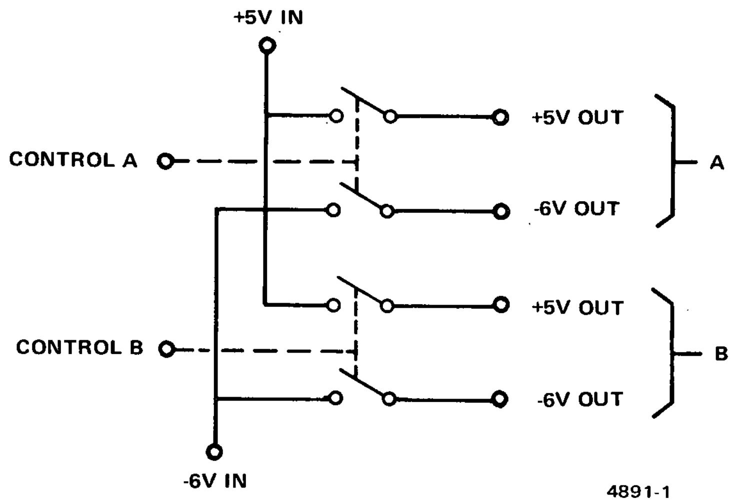


Figure 19. Power Switch +5 V/ -6 V

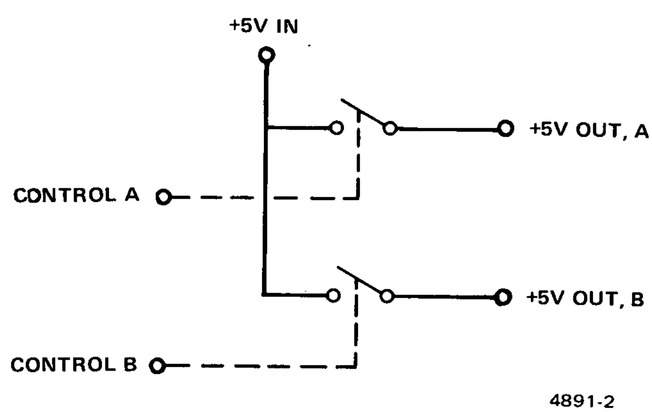


Figure 20. Power Switch +5 V/+5 V

Each carrier structure contains 64 word lines and 100 bit lines (plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the polyimide film which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the carrier structure is shown in Figure 21.

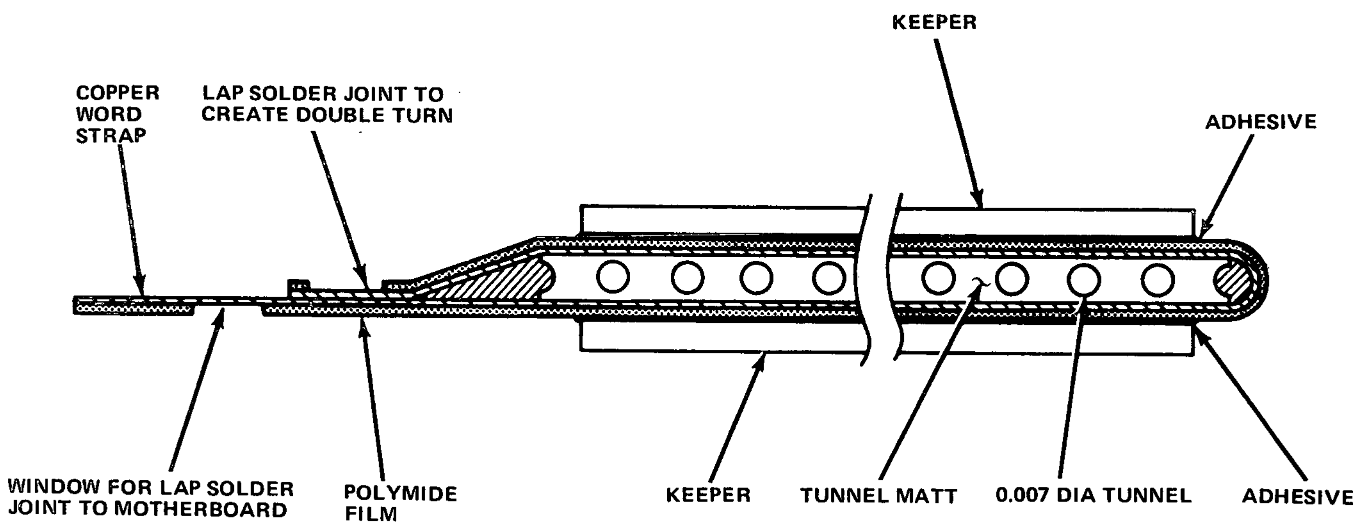


Figure 21. Carrier Structure Construction

3.5.1.2 Memory Plane

The memory plane is fabricated by laminating two carrier structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a conductor pattern to match the carrier structure word line pattern in the "window" area. A lap solder joint in this window connects the word lines to the 8 x 8 word drive matrix on the motherboard. The input and return for the matrix is tracked to the edge of the board where flat flexible conductor is used to interface with the plane. Two carrier structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly.

3.5.1.3 Plated Wire Stack

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

Flexible circuitry is also used to interconnect common word drive signals from plane to plane and, combined with miniature connectors, carry all digit and word signals to the electronics. The use of flex circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.

During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board was located on top of the plated wire stack while the two digit drive/sense boards were located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction. The memory internal assembly is shown in Figure 1.

The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.3" wide and contains 6 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 4.5" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Six special high strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from aluminum. The Memory housing is 9.0" long x 5.8" wide x 2.8" high (exclusive of mounting flanges and connectors) establishing a volume of 126 cubic inches. The system has a total weight of 5.4 pounds.

3.5.3 Materials

Motorola's basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner'71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. The use of any material is dependent not only on the material but also on its receiving the proper processing and cure. This factor was considered in the assembly procedures and processes used to fabricate the memory system.

All of the materials used in the LP RASM were submitted to the Chemistry and Physics Section of the Engineering Physics Division at GSFC for review and approval. From the preliminary design, some alternate materials were recommended and some changes in cure cycles were suggested. If data was not readily available on a material it was tested by the C&P Section to insure it met all requirements.

SECTION 4

TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its components at the piece part level and at each level of assembly. The formal test documents for tests performed at the stack and system levels are included as appendices.

4.1 SYSTEM LEVEL TESTING

Both Acceptance and Qualification tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of $+85^{\circ}C$ and $-40^{\circ}C$. The Acceptance Test Procedure and Test Data Records are included as Appendix I Acceptance Tests (except at high and low temperatures) were repeated after qualification testing.

Qualification testing consisted of both sine and random vibration, shock and altitude (to 10^{-5} mm Hg). The memory unit was continuously exercised during all qualification testing. The Qualification Test Procedure and Data Records are included as Appendix II.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive, worst-case tests, over temperature, at the stack level using an EH8500 computer controlled memory tester. These tests were performed in accordance with a formal stack test procedure, which is included as Appendix III. The procedure is quite definitive, however, and some explanation is probably in order relative to the test pattern shown in Figure 5 (page 10 of the test procedure).

The first three horizontal rows relate to word current in the word line corresponding to the particular bit under test and word currents in the two word lines immediately adjacent (i.e., left adjacent bit and right adjacent bit). The fourth row relates to digit current in the plated-wire corresponding to the particular bit under test.

The vertical columns relate to successive time slots, left-to-right except that, as indicated in the row labeled NO. OF CYCLES, the first group of three time slots is cycled through 10^3 times before stepping to the fourth time slot.

IWD identifies a maximum, or disturb, word current level. IWW and IWR identify a minimum word current level, which is worst-case for writing and reading in the bit-under-test. IDD1 and IDD2 identify maximum, or disturb, bipolar digit current levels. IDW1 and IDW2 identify minimum levels of the bipolar digit currents. These are worst-case for writing in the word-under-test.

During the first three time slots, information of a particular polarity is "hard-written" (i.e., under maximum word and digit current levels) into the bit-under-test and its two adjacent bits along the same plated-wire. This is done 1000 times and constitutes adverse history.

The opposite polarity information is then "soft-written" one time in the bit-under-test and then immediately read out, again with minimum word current. The resulting wire output represents an "undisturbed" condition (i.e., with no intervening activity at adjacent bit locations).

The next four program steps are cycled through a total of 10,000 times. During the first time slot, information opposite to that stored in the bit-under-test is written into one of the adjacent bits under conditions of worst-case maximum word and digit current levels. In the second time slot, maximum-level word current is pulsed through the word line corresponding to the bit-under-test. The same two steps are then repeated, only with reference to the other adjacent bit.

During the final time period, the bit-under-test is again read and compared to preset limits, using worst-case minimum word current.

Any wire which did not meet a minimum output level requirement of 5.0 millivolts, over temperature, was replaced. This amounted to a total of 35 wire pairs. There is a total of 576 wire pairs (72 pairs per plane times 8 planes) in the stack. The replacement incidence therefore represented approximately 6 percent, which is well within normal expectations.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100 percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included precap visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging and leak testing. (As mentioned previously, operational vibration and power aging requirements were waived on a total of 138 hybrid circuits manufactured for the final design configuration).

APPENDIX I

ACCEPTANCE TEST PROCEDURES

Item 2

APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	INITIAL RELEASE	2-1-71	LB
X2	Changed -6.2 V. to -6.5V. Added interleaved read/write test. Deleted references to +15V	1-16-72	HRT
X3	Retyped to Incorporate Procedural changes and corrections. Changed -6.2V to -6.9V.	4-17-72	HRT

REV																					
SHEET																					
REV STATUS	REV	X1	X1	X1	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X3	X2	X3
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY	S. Hueske
CHK BY	B. Lott
MFG	PROJ NO. 3917
CONTR NO.	NAS5-20155
RELEASE NOTICE	
APPROVED	E Anker — DATE 2-1-71
APPROVED	Larry L Bro — DATE 2-1-71

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST PROCEDURE LOW POWER RANDOM ACCESS SPACECRAFT MEMORY
PART NO. 01-P13666B

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P11215B

SCALE | SHEET 1 OF 20

I-1

AV-1-B-199H-100A-3/69 DWG FORMAT

TABLE OF CONTENTS

1.0 SCOPE

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13666B, manufactured under Contract No. NAS5-20155.

2.0 REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P11173B	Motorola Plated Wire Memory Tester Operating Manual.

2.2 DEFINITIONS

1	UP position on DATA and ADDRESS switches, DATA and ADDRESS lamps ON
0	DOWN position on DATA and ADDRESS switches, DATA and ADDRESS lamps OFF
Tester	Motorola Plated Wire Memory Tester
MSB	Most Significant Bit
LSB	Least Significant Bit
Error Lamps	Lamp ON indicated ERROR present.

3.0 TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

ITEM	MANUFACTURER	MANUFACTURER'S MODEL OR TYPE	RANGE & ACCURACY
DC Milliammeter	Hewlett Packard	428BR	0-10 Amp.
Oscilloscope	Tektronix	585	50ns/cm
Scope Plug-In	Tektronix	82	Tr 1.5ns
Digital Voltmeter	Hewlett-Packard	3440A	Accuracy ± .05% of reading
Counter	CMC	727BN	0.1% ± 1/2 LSB
DC Multifunction Unit	Hewlett-Packard	3444A	0-999.9 ma. 0-9.999 megohms
Oven	Wyle	CO-106-1800	-100°F to +500°F
Power Supplies	Precision Design Inc	5015-A	0-50V, 1.5 Amp.
Power Supplies	Precision Design Inc.	5015-S	0-50V, 1.5 Amp.
Pulse Generator	EH	139B	10Hz to 50MHz

NON-STANDARD TEST EQUIPMENT

(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-P11170B001

NOTE: The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE: The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull up resistor to signals coming back from the memory.

3.2 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions.

3.2.1 Power Supply Voltage

The unit specified to be tested shall operate from the following DC source voltages, +5V ± 5%, and -6.9V ± 5%.

3.2.2 Ambient Temperature

The unit shall be tested in a laboratory area having temperature of 25 ± 10°C (77 ± 18°F).

3.2.3 Ambient Humidity

Normal laboratory ambient, not to exceed 90%.

3.2.4 Ambient Atmospheric Pressure

Normal laboratory ambient.

3.2.5 Shielding and Isolation Requirements

No special precautions are required.

3.2.6 Stabilization Period

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

3.2.7 Cooling

None required.

4.0 PHYSICAL CHARACTERISTICS

The volume and weight of the LP RASM are to be measured.

4.1 WEIGHT

Place the LP RASM on the scale and read and record in the data sheet the weight of the memory in pounds.

4.2 DIMENSIONS

Measure and record in the data sheet the outside dimensions as shown in Figure 1. Compute and record in the data sheet the memory volume by multiplying dimension W by dimension H by dimension D. (V = W X H X D).

5.0 ELECTRICAL TESTS

5.1 ELECTRICAL TEST EFFORT

The electrical test effort shall consist of a Functional Test (5.4), and Temperature Test (6.0).

5.2 TEST LOG

This test log shall be used to record the history of the memory starting from the first system test. It shall show all testing, rework and idle time of the memory.

5.3 INTERCONNECTION

All the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for +3 ± 0.1V positive pulses of 450 ± 10 nanosecond duration (at the 50 percent points) at a 500 ± 1.0 KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

5.4 FUNCTIONAL TESTS

5.4.1 Preliminary Control Settings

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
Tester	
BD 1-BD4 (24 Swtiches)	No. 0 Down all Others Up
Tape Reader Power	Light Off
Run-Off-Rewind Switch	Off
Tester Power	Light On
Address Switches	Down
Data Switches	Down
Read/Write	WRITE
Word Length	24
Read 1/Read 7 Switch	READ 1
Address Pattern	SEQ.
Data Pattern	MAN
Frequency	EXT.
Interface Box	
Memory Select Switches	All 2.4V
Input Current Switch	GND
Output Pullup Resistor	GND
WC Switch	Off
Initiate Pulse Switch	GND
WC2 Switch	Off
Memory Power	Off

5.4.1.1 Initial Power Supply Conditions

Using the DVM, adjust the three supplies as follows:

+5V to Interface Box: +5.0 ± 0.1V

+5V to Memory: +5.0 ± 0.1V

-6.9V to Memory: -6.9 ± 0.1V

Set the meter selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

5.4.2 Chassis Isolation

Using the digital ohmeter verify that the impedance between the memory chassis and ground test point on the interface box is ≥ 9 megohoms. Record the results in the Data Sheet.

5.4.3 Input Signal Loading

5.4.3.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).

5.4.3.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.

5.4.3.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter. Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position. Momentarily set MEMORY POWER to ON and measure and record

the current.
Disconnect the ammeter and replace the jumper wire. Set the MEMORY SELECT 1 SWITCH back to the +2.4V position.

5.4.3.4 Repeat paragraph 5.4.3.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.

5.4.3.5 Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.

5.4.3.6 Connect the ammeter between the ADDRESS BIT 2^0 and the INPUT CURRENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current.
Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.
Repeat the above two measurements at each of the 12 address bit test points.
Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).
Verify that thet MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

5.4.4 <u>Verification of Open Collector on Output Signals</u>

5.4.4.1 Connect the Interface Box to the tester. Connect the -6.9V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons.

5.4.4.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "0" in all data bits in all 4096 addresses one time and stop.

5.4.4.3 Set the READ/WRITE switch on the tester to the READ position. Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be ≤ 100 mv.

(The read complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

5.4.4.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be ≤ 100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.

5.4.5 Power Consumption

5.4.5.1 Using the DVM, adjust the +5V and -6.9V memory power supplies to +5.0 ± 0.1V and -6.9 ± 0.1V, respectively. Record the voltages.

Using the 428BR milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

5.4.5.2 Deleted. (+15V Power Measurement).

5.4.5.3 Using the milliammeter, measure and record the current to the -6.9V supply. Compute and record the -6.9V power.

5.4.5.4 Compute and record the total Memory Idle Power.

5.4.5.5 Set the ADDRESS PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.

5.4.5.6 Repeat 5.4.5.1.

C.2

5.4.5.7 Deleted. (+15V Power Measurement).

5.4.5.8 Repeat 5.4.5.3.

5.4.5.9 Compute and record the Total Active Power.

5.4.6 Read Complete Timing

5.4.6.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to INITIATE PULSE test point, channel B voltage probe to READ COMPLETE test point.

5.4.6.2 Set DATA PATTERN switch to MAN.

5.4.6.3 Set READ/WRITE switch to READ.

5.4.6.4 Depress and release the RESET button, then the START button.

5.4.6.5 Synchronize the oscilloscope on the leading edge of the initiate pulse.

5.4.6.6 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points.) Record the pulse delay and duration in the data sheet.

5.4.7 System Function Tests

5.4.7.1 Depress and release RESET button. Set ADDRESS PATTERN switch to SEQ. Set DATA PATTERN switch to SEQ.

5.4.7.2 Depress and release START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1", reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs.

Record any errors.

Test for 10 seconds. Use the counter to measure the elapsed test time.

Depress the STOP button.

5.4.7.3 Set READ 1/READ 7 Switch in the READ 7 position. The READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "1", read a "1", seven times in each memory locations.

5.4.7.4 Depress and release the START button. The Tester continues to cycle unless an error occurs.

Record any errors.

Test for 10 seconds.

5.4.7.5 Depress and release the STOP button.

5.4.7.6 Set DATA PATTERN switch to MAN.

5.4.7.7 Set READ-WRITE switch to WRITE.

5.4.7.8 Set all DATA switches to UP position. Depress and release RESET button.

5.4.7.9 Depress and release START button. Memory will cycle thru all 4096 addresses one time and stop.

5.4.7.10 Set READ-WRITE switch to READ. Depress and release RESET button.

5.4.7.11 Depress and release START button. Run for one minute. Record any errors.

5.4.7.12 Depress and release STOP button.

5.4.7.13 Set READ-WRITE switch to WRITE.

5.4.7.14 Set all DATA switches to DOWN position. Depress and release RESET button.

5.4.7.15 Depress and release START button. Memory will cycle thru all 4096 addresses one time and stop.

5.4.7.16 Set READ-WRITE switch to READ. Depress and release RESET button.

5.4.7.17 Depress and release START button. Run for one minute. Record any errors.

5.4.7.18 Depress and release STOP button.

5.4.8 Random Access Capability

5.4.8.1 Set READ-WRITE switch to WRITE.

5.4.8.2 Set ADDRESS PATTERN switch to MAN.

5.4.8.3 Select an address at random with the ADDRESS switches.

5.4.8.4 Set DATA switches in a random pattern. Depress and release RESET button.

5.4.8.5 Depress and release START button. The selected data will be written into the selected address.

5.4.8.6 Depress and release the Stop button. Set the READ-WRITE switch to READ.

5.4.8.7 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.

5.4.8.8 The operator should select 3 other addresses at random repeating steps 5.4.8.1 thru 5.4.8.7 and verify that the unit indeed does have random access capability.

5.4.9 Non-Volatility Test

5.4.9.1 Set ADDRESS PATTERN switch to SEQ.

5.4.9.2 Set DATA PATTERN switch to MAN. Set DATA switches to a random pattern. Depress and release RESET button. Set READ-WRITE switch to WRITE.

5.4.9.3 Depress and release START button. The tester will run through all 4096 addresses one time and then stops.

5.4.9.4 Turn memory power off.

5.4.9.5 Set READ-WRITE switch to READ.

5.4.9.6 Depress and release the RESET button.

5.4.9.7 Turn memory power on.

5.4.9.8 Depress and release the START button. If an error occurs, record this on the data sheet. If no error occur, no words were disturbed when the power was interrupted.

5.4.9.9 Depress and release the STOP button.

5.4.10 <u>Memory Select Test</u>

5.4.10.1 Set ADDRESS PATTERN switch to SEQ and DATA PATTERN switch to SEQ.

5.4.10.2 Set Memory Select switches to "0000".

5.4.10.3 Depress and release RESET button, then the START button. Tester shall indicate an error at the first address. Record the address on the data sheet.

5.4.10.4 Repeat 5.4.10.3 with memory select switches set to "0001", "0010", "0011", "0100", "0101", "0110", "0111", "1000", "1001", "1010", "1011", "1100", "1101", and "1110".

5.4.10.5 Set MEMORY SELECT switches to "1111".

5.4.10.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow tester to run for 10 seconds. Record any errors. Depress and release the STOP button.

5.4.11 __Worst Case Pattern Test__

5.4.11.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WC1. Turn the WC switch ON. Depress and release the STOP and RESET buttons.

5.4.11.2 Depress and release the START button. The tester will execute the following sequence:

a. Write a "1" in every bit of every word 2^{10} times.

b. Write a "0" once in every bit of every word under an even numbered word line in the stack.

c. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.

NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worst-case pattern tests.

Run in cycle C for one minute. Record any errors on the data sheet.

5.4.11.3 Press and release the WC1 SEQ button. The tester will execute the preceeding sequence except "even" and "odd" are interchanged. The $WC2^0$ and $WC2^1$ lights will indicate the second WC1 group is under test. Record any errors.

5.4.11.4 Repeat 5.4.11.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet. Depress and release the STOP button. Turn the MEMORY POWER off.

6.0 TEMPERATURE TEST

6.1 TEMPERATURE TEST SETUP

6.1.1 The temperature tests shall be conducted under normal laboratory conditions with the exception of temperature.

6.2 THERMAL CYCLE

6.2.1 Place the unit in the temperature chamber and re-establish the test setup as shown in Figure 2.

6.2.2 High Temperature

Increase the environmental temperature to 85°C ± 3°C. Beginning 50 minutes after the temperature chamber has reached 85°C, measure and record in the data sheet thermistor resistance at 10 minute intervals. Do this by placing the digital ohmmeter across the THERMISTOR terminals on the interface box. At each measurement, except the first one, calculate the percent change from the previous reading. When the percent change is ≤ 10%, proceed to paragraph 6.2.2.1.

6.2.2.1 Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ. Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -7.25 ± 0.02V.

Measure and record the power supply voltage, current and standby (idle) power (paragraphs 5.4.5.1 through 5.4.5.4, except do not readjust the voltages).

6.2.2.2 Depress the START button. The memory shall run without error for 10 seconds. Record the results.

6.2.2.3 Measure and record the operating power (paragraphs 5.4.5.6 through 5.4.5.9, except adjust the voltages to +5.25 ± 0.02V and -7.25 ± 0.02V).

Depress the STOP button.

6.2.2.4 Repeat paragraphs 5.4.11.1 through 5.4.11.4.

6.2.2.5 Set the MEMORY POWER switch to ON.

Set the +5V supply to 5.0V ± .02 and the -6.9V supply to -6.9 ± .02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory will run without error. After 10 seconds, push the STOP button. Set MEMORY POWER to OFF.

6.2.3 <u>Low Temperature</u>

Remove the oven door and let the memory unit cool to approximately room temperature. Place the memory unit in a plastic bag and again seal the chamber.

Decrease the environmental temperature to -40°C ± 3°C. Beginning 150 minutes after the temperature chamber has reached -40 C, measure and record in the data sheet thermistor resistance at 10 minute intervals. Do this by placing the digital ohmmeter across the THERMISTOR terminals on the interface box. At each measurement, except the first one, calculate the percent change from the previous reading. When the precent change is ≤ 5%, proceed to paragraph 6.2.3.1.

6.2.3.1 Depress the START button. The memory shall run without error for 10 seconds. Depress the STOP button and record the results.

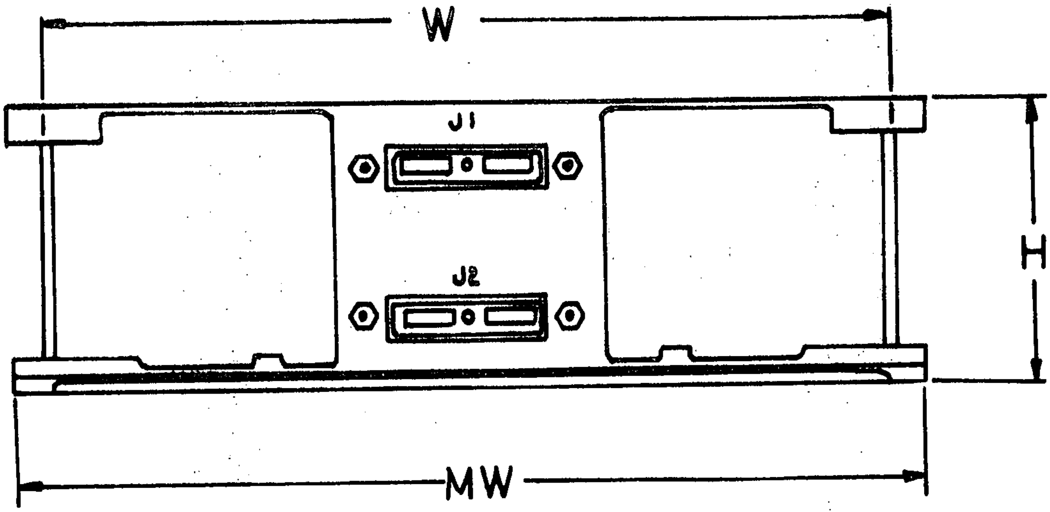
6.2.3.2 Set the +5V supply to 5.25V ± .02V and the -6.9V supply to -7.25 ± .02V. Measure and record the power supply volt & the standby power (paragraphs 5.4.5.1 through 5.4.5.4, except do not readjust the voltages).

6.2.3.3 Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record in the data sheet the operating power (paragraphs 5.4.5.6 through 5.4.5.9 except adjust the voltages to +5.25 ± 0.02V and -7.25 ± 0.02V).

6.2.3.4 Set the +5V supply to 4.75 ± .02V and the -6.9V supply to -6.55 ± .02V. Push the RESET pushbutton. The memory shall run without error for one minute. Record the results in the data sheet.

6.2.3.5 Repeat paragraphs 5.4.11.1 through 5.4.11.4.

Turn the memory power OFF.



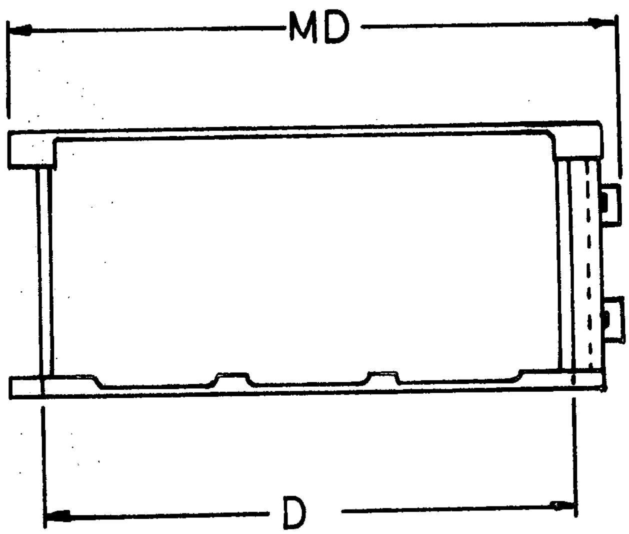


FIGURE 1. LP RASM OUTLINE DIMENSIONS

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11215B	
	SCALE NONE		REVISION X2	SHEET 19

AV-2-B-199H-100A-3/69 DWG FORMAT

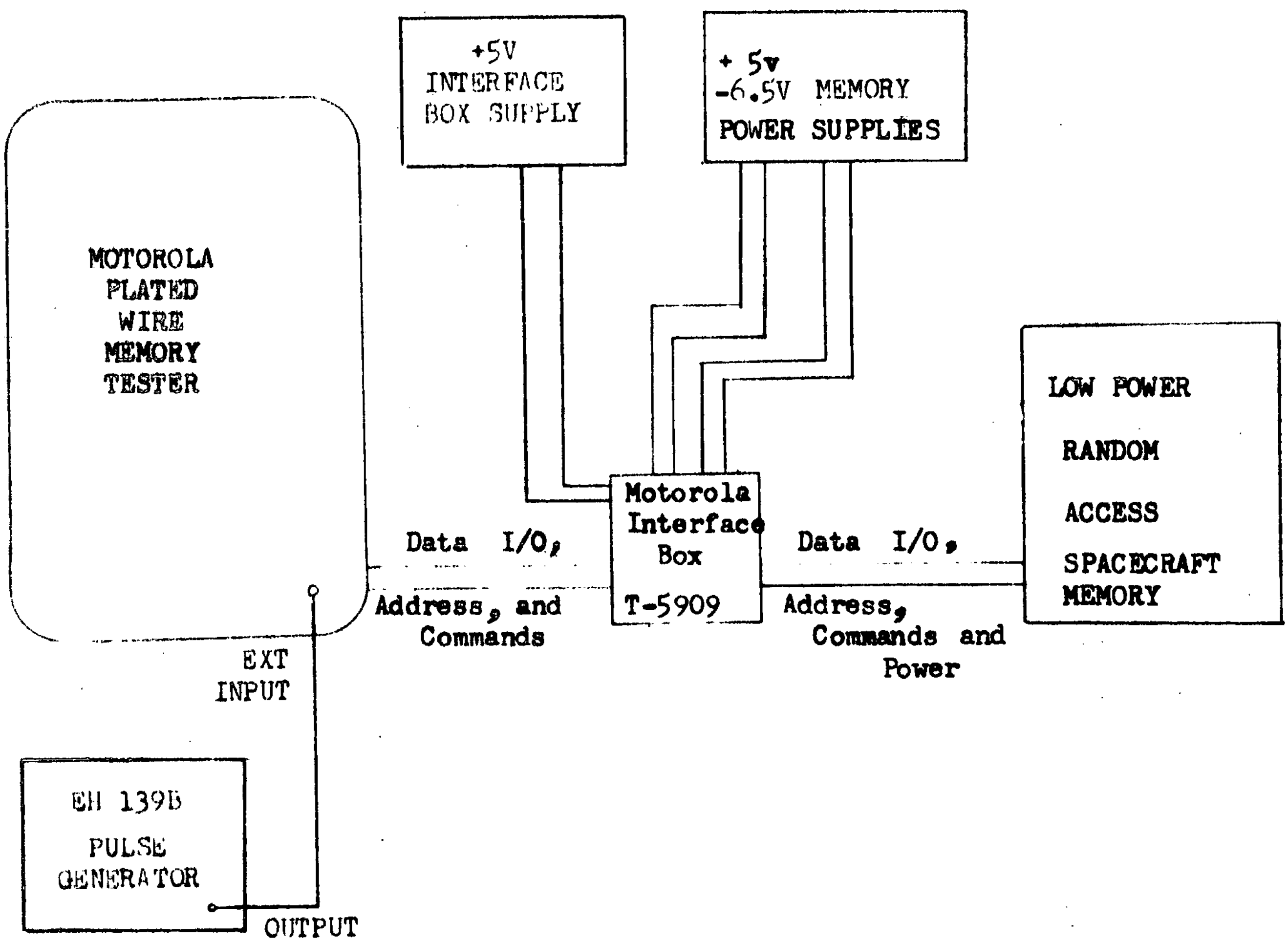


FIGURE 2. ELEC TEST INTERCONNECT DIAGRAM

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11215B	
	SCALE	REVISION X3		SHEET 20

AV-2-B-199H-100A-3/69 DWG FORMAT

APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	INITIAL RELEASE	2-1-71	EB
X2	Changed -6.2V to -6.5V. Added interleaved read-write test. Changed operating power to 7W. Deleted references to +15V.	1-16-72	HRT
X3	Updated for compatibility with Rev. X3 of the ATP.	4-17-72	HRT

PRE-QUALIFICATION TEST DATA

REV																		
SHEET																		
REV STATUS	REV	X3	X3	X3	X1	X3	X1	X3	X3	X3	X1	X3	X3	X2	X3	X3	X3	X3
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY S. Hueske

CHK BY B. Lott

MFG

PROJ NO. 3917

CONTR NO. NAS5-20155

RELEASE NOTICE

APPROVED [illegible] DATE 2-1-71

APPROVED [illegible] DATE 2-1-71

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST PROCEDURE TEST DATA SHEET - LOW POWER RANDOM ACCESS SPACECRAFT MEMORY PART NO. 01-P13666B

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P11216B

SCALE

SHEET 1 OF 17

AV-1-B-1998-100A-3/69 DWG FORMAT

1.0 SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory 12-P11215B.

2.0 REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P11215B	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3.0 TEST DATA

Unit S/N 001

Date of Test 4-14-72

Tested By

WITNESSED BY: CLAUDE DOCHOW

ATP Para No.

3.1 EQUIVALENT TEST EQUIPMENT

4.0 PHYSICAL CHARACTERISTICS — Limit

4.1 WEIGHT

Weight of LP-RASM = 5.41 pounds P.E.C. 5.5 pounds

4.2 DIMENSIONS

H = 2.860 inches

W = 8.371 inches

MW = 8.971 inches

P.E.C.

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P11216B
	SCALE	REVISION X3	SHEET 2

AV-2-B-1591-100A-3.69 DWG FORMAT

S/N 001 | Date of Test 4-19-72

Tested By H. Lund

WITNESSED BY: CLAUDE DOCHAM

Limit

D = 5.273 inches

MD = 6.291 inches

V = H X W X D = 126.25 $inches^3$ P.E.C. ≤ 127 $inches^3$

5.4.2 Chassis Isolation

Impedance >9 MEG Ω ≥9 megohms

5.4.3 Input Signal Loading

5.4.3.2 Current from INITIATE PULSE to Gnd .98 ma ≤2 ma

Current from 2.4V to INITIATE PULSE 1.9 μa ≤20 μa

5.4.3.3 Current from MEM SEL 1 to Gnd .96 ma ≤2 ma

Current from 2.4V to MEM SEL 1 1.1 μa ≤20 μa

P.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 3

AV-2-B-1991I-100A-3/69 DWG FORMAT

WITNESSED BY: CLAUDE DOCHOW

S/N 001

Date of Test 4-19-72

Tested By H. [signature]

P.E.C.

		Measured	Units	Limits
5.4.3.4	Current from MEM SEL 2 to Gnd	.96	ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.2	μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	.96	ma	≤ 2 ma
	Current from 2.4V to MEM SEL 3	1.2	μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	.96	ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	1.3	μa	≤ 20 μa
5.4.3.5	Current from READ/WRITE to Gnd	.98	ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	7.9	μa	≤ 20 μa
5.4.3.6	Current from ADDRESS 2^0 to Gnd	.89	ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	.49	μa	≤ 20μa
	Current from ADDRESS 2^1 to Gnd	.89	ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^1	.38	μa	≤ 20μa
	Current from ADDRESS 2^2 to Gnd	.89	ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^2	.57	μa	≤ 20μa
	Current from ADDRESS 2^3 to Gnd	.89	ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^3	.37	μa	≤ 20μa
	Current from ADDRESS 2^4 to Gnd	.89	ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^4	.47	μa	≤ 20μa

P.E.C.

WITNESSED BY: CLAUDE DOCHOM

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.C.

			Limits
Current from ADDRESS 2^5 to Gnd	.90	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.48	μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	~~1.0~~	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	~~.92~~	μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^6	.92	μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	.9	μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.0	μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.0	μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	.8	μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	.8	μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	.8	μa	≤ 20μa

HRT CD REDUNDANT P.E.C.

P.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 5

AV-2-B-1598-100A-3/69 DWG FORMAT

WITNESSED BY: CLAUDE DOCHW

S/N 001

Date of Test 4-19-72

Tested By H. Sund

P.E.C.

			Limits
Current from DATA IN BIT 1 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	.9	µa	≤ 20 µa
Current from DATA IN BIT 2 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	.8	µa	≤ 20 µa
Current from DATA IN BIT 3 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	.8	µa	≤ 20 µa
Current from DATA IN BIT 4 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	.9	µa	≤ 20 µa
Current from DATA IN BIT 5 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	.8	µa	≤ 20 µa
Current from DATA IN BIT 6 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	.8	µa	≤ 20 µa
Current from DATA IN BIT 7 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	.8	µa	≤ 20 µa
Current from DATA IN BIT 8 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	.8	µa	≤ 20 µa
Current from DATA IN BIT 9 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	.8	µa	≤ 20 µa

P.E.C.

WITNESSED BY: CLAUDE DOCHOW

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.C.

			Limits
Current from DATA IN BIT 10 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	.8	μa	≤ 20 μa
Current from DATA IN BIT 11 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	.8	μa	≤ 20 μa
Current from DATA IN BIT 12 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	.8	μa	≤ 20 μa
Current from DATA IN BIT 13 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 13	.8	μa	≤ 20 μa
Current from DATA IN BIT 14 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	.8	μa	≤ 20 μa
Current from DATA IN BIT 15 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	1.1	μa	≤ 20 μa
Current from DATA IN BIT 16 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 16	1.0	μa	≤ 20 μa
Current from DATA IN BIT 17 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	1.1	μa	≤ 20 μa

P.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 7

V-2-B-1991-100A-3/69 DWG FORMAT

WITNESSED BY: CLAUDE DOCHOW

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.C.

5.4.4 Verificatin of open collector on output signals

				Limit
5.4.4.3	READ COMPLETE voltage	<75	mv	≤100 mv
5.4.4.4	DATA OUT BIT 0 voltage	50	mv	≤100 mv
	DATA OUT BIT 1 voltage	75	mv	≤100 mv
	DATA OUT BIT 2 voltage	75 ~~50~~	mv P.E.C.	≤100 mv
	DATA OUT BIT 3 voltage	50	mv	≤100 mv
	DATA OUT BIT 4 voltage	50	mv	≤100 mv
	DATA OUT BIT 5 voltage	75	mv	≤100 mv
	DATA OUT BIT 6 voltage	75	mv	≤100 mv
	DATA OUT BIT 7 voltage	50	mv	≤100 mv
	DATA OUT BIT 8 voltage	50	mv	≤100 mv
	DATA OUT BIT 9 voltage	75	mv	≤100 mv
	DATA OUT BIT 10 voltage	75	mv	≤100 mv
	DATA OUT BIT 11 voltage	75	mv	≤100 mv
	DATA OUT BIT 12 voltage	75	mv	≤100 mv
	DATA OUT BIT 13 voltage	75	mv	≤100 mv
	DATA OUT BIT 14 voltage	85	mv	≤100 mv
	DATA OUT BIT 15 voltage	50	mv	≤100 mv
	DATA OUT BIT 16 voltage	75	mv	≤100 mv
	DATA OUT BIT 17 voltage	85	mv	≤100 mv

P.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 8

AV-2-B-199H-100A-3/69 DWG FORMAT

WITNESSED BY: [illegible]

S/N 001	Date of Test 4-19-72
	Tested By H. [illegible]
	P.E.O.

5.4.5 Power Consumption (25°C) — Limits

5.4.5.1	Memory +5v current	~~30~~ 16.4 cd (M 983)	ma P.E.O.	
	Memory +5v power	82.0	mw	
	+5V Voltage	5.0	Volts	
5.4.5.2	DELETED.			
5.4.5.3	Memory -6.9V current	1.8	ma	
	Memory -6.9V power	12.42	mw	
	-6.9V Voltage	-6.9	Volts	
5.4.5.4	Memory idle total power	94.42	mw	≤ 150 mw
5.4.5.6	Memory +5v current	540	ma	
	Memory +5v power	2700	mw	
5.4.5.7	DELETED.			
5.4.5.8	Memory -6.9V current	143	ma	
	Memory -6.9V power	986.7	mw	
	-6.9V Voltage	6.9	volts	
5.4.5.9	Total active power	3687	mw	≤ 6000 mw

5.4.6 Read Complete Timing

5.4.6.6	Delay	295	ns	≤ 500 ns
	Duration	285	ns	250 ns min. 450 ns max.

P.E.Q.

WITNESSED BY: CLAUDE DOCHON

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.O.

5.4.7 System Function Test Limits

5.4.7.2 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.7.4 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.7.11 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.7.17 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.8 Random Access Capability

5.4.8.7 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.8.8 Did an error occur?

a) No X

Yes ____ Address ____ Bits ____ 0 errors

G.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X1	SHEET 10

AV-2-B-1991I-100A-3/69 DWG FORMAT

WITNESSED BY. CLAUDE DOCHON

S/N 001

Date of Test 4-19-72

Tested By H. Lined

P.E.G

Limits

b) No X

Yes ____ Address ____ Bits ____ 0 errors

c) No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.9 Non-Volatility Test

5.4.9.8 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

5.4.10 Memory Select Test

				Limits
5.4.10.3	Address		0000 (Octal)	0000
5.4.10.4	Address	0001	0000 (Octal)	0000
		0010	0000 (Octal)	0000
		0011	0000 (Octal)	0000
		0100	0000 (Octal)	0000
		0101	0000 (Octal)	0000
		0110	0000 (Octal)	0000
		0111	0000 (Octal)	0000
		1000	0000 (Octal)	0000
		1001	0000 (Octal)	0000
		1010	0000 (Octal)	0000

P.E.C.

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION X3	SHEET 11

WITNESSED BY: CLAUDE DOCHOW

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.C.

				Limits
Address	1011	0000	(Octal)	0000
	1100	0000	(Octal)	0000
	1101	0000	(Octal)	0000
	1110	0000	(Octal)	0000

5.4.10.6 Did an error occur?

No X

Yes ______ Address ______ Bits ______ 0 errors

5.4.11 Worst Case Pattern Test

5.4.11.2 Did an error occur?

No X

Yes ______ Address ______ Bits ______ 0 errors

5.4.11.3 Did an error occur?

No X

Yes ______ Address ______ Bits ______ 0 errors

P.E.C.

WITNESSED BY: CLAUDE DOCHOIN

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.C.

Limits

5.4.11.4 a) Did an error occur?

No X

Yes ______ Address ______ Bit ______ 0 errors

b) Did an error occur?

No X

Yes ______ Address ______ Bit ______ 0 errors

P.E.C.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X2	SHEET 13

AV-2-B-199H-100A-3 69 DWG FORMAT

WITNESSED BY: CLAUDE DOCHON

S/N 001

Date of Test 4-19-72

Tested By H. Lund

P.E.O.

Limits

6.2 THERMAL CYCLE

6.2.2 High Temperature

Thermal Resistance

50 minutes 1.913 K ohms

60 minutes 1.754 K ohms % change 8.3%

70 minutes — K ohms % change —

80 minutes — K ohms % change —

90 minutes — K ohms % change —

6.2.2.1 +5V current 19.0ma

-6.9V current 4.2 ma Total power 130.2mw ≤150 mw

+5V Voltage 5.25

-6.9 V Voltage -7.25

6.2.2.2 Did an error occur?

No X

Yes ______ Address ______ Bit ______ errors

6.2.2.3 -6.9V voltage -7.25 volts +5V current 665 ma

+5.0V voltage 5.25 volts

-6.5V current 249 ma Total Power 5289 mw ≤6000 mw

6.2.2.4 WC a) Did an error occur?

No X

Yes ______ Address ______ Bits ______

P.E.O.

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P11216B
	SCALE	REVISION X3	SHEET 14

A7-2-B-1938-100A-3 69 DWG FORMAT

WITNESSED BY: CLAUDE DOCHOV

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

P.E.O.

WC b) Did an error occur?

No X

Yes ____ Address ____ Bits ____

WC c) Did an error occur?

No X

Yes ____ Address ____ Bits ____

WC d) Did an error occur?

No X

Yes ____ Address ____ Bits ____

6.2.2.5 Did an error occur?

No X

Yes ____ Address ____ Bits ____

P.E.C.

6.2.3 Low Temperature

Thermal Resistance

150 minutes	6800	K ohms		
160 minutes	7226	K ohms	% change	6.17%
170 minutes	7602	K ohms	% change	5.21%
180 minutes	8007	K ohms	% change	5.33%
190 minutes	8404	K ohms	% change	4.95%

6.2.3.1 Did an error occur?

No X

Yes ____ Address ____ Bits ____

WITNESSED BY: CLAUDE DOCHOW

S/N 001

Date of Test 4-19-72

Tested By H. [signature]

				Limits
6.2.3.2		+5V current 21 ma		Power Supply
	-6.9V current 5.3 ma	Total power 149 mw		≤150 mw
		+5V Voltage 5.25		
	-6.9V voltage - 7.25			
6.2.3.3		+5V current 605 ma		
	-6.9V current 244 ma	Total power 4945 mw		≤6000 mw

6.2.3.4 Did an error occur?

No X

Yes _____ Address _____ Bits _____

6.2.3.5 WC a) Did an error occur?

No X

Yes _____ Address _____ Bits _____

WC b) Did an error occur?

No X

Yes _____ Address _____ Bits _____

[signature]

MOTOROLA INC. Government Electronics Division 8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 16

AV-2-0-159H-100A-3.69 DWG FORMAT

S/N 001

Date of Test 4-19-72

Tested By H. [illegible]

WITNESSED BY: CLAUDE DOCHOW

WC c) Did an error occur?

No X

Yes ______ Address ______ Bits ______

WC d) Did an error occur?

No X

Yes ______ Address ______ Bits ______

MRI

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P1121GB
	(The reverse of this page is blank.)		SHEET 17

AE 9 D 10-4 100A 3/69 DWG FORMAT

APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	INITIAL RELEASE	2-1-71	RB
X2	Changed -6.2V to -6.5V. Added interleaved read-write test. Changed operating power to 7W. Deleted references to +15V.	1-16-72	HRT
X3	Updated for compatibility with Rev. X3 of the ATP.	4-17-72	HRT

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POST-QUALIFICATION TEST DATA PER INSTUCTIONS OF PARAGRAPH 9.0 OF QUALIFICATION TEST PROCEDURE 12-P13675B, REV. X4.

REV STATUS OF SHEETS																		
REV	X3	X3	X3	X1	X3	X1	X3	X3	X3	X1	X3	X3	X2	X3	X3	X3	X3
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY S. Hueske

CHK BY B. Lott

MFG

PROJ NO. 3017

CONTR NO. NAS5-20155

RELEASE NOTICE

APPROVED [illegible] DATE 2-1-71

APPROVED [illegible] DATE 2-1-71

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST PROCEDURE TEST DATA SHEET - LOW POWER RANDOM ACCESS SPACECRAFT MEMORY PART NO. 01-P13660B

SIZE A | CODE IDENT NO. 94990 | DWG. NO. 12-P11216B

SCALE | SHEET 1 OF 17

AV-1-B-1591-10JA-3.69 DWG FORMAT

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1.0 SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory 12-P11215B.

2.0 REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P11215B	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3.0 TEST DATA

Unit S/N 001 Date of Test 5-3-72

Tested By [signature]

ATP Para No.

3.1 EQUIVALENT TEST EQUIPMENT

4.0 PHYSICAL CHARACTERISTICS Limit

4.1 WEIGHT

Weight of LP-RASM = 5.45 pounds 5.5 pounds

4.2 DIMENSIONS

H = 2.858 inches

W = 8.372 inches

MW = 8.969 inches

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 2

S/N 001

Date of Test 5-3-72

Tested By H. [illegible]

			Limit
D =	5.276	inches	
MD =	6.290	inches	
V = H X W X D =	126.25	$inches^3$	≤ 127 $inches^3$

5.4.2 Chassis Isolation

			Limit
Impedance	>9		≥ 9 megohms

5.4.3 Input Signal Loading

5.4.3.2	Current from INITIATE PULSE to Gnd	0.98	ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	1.6	μa	≤ 20 μa
5.4.3.3	Current from MEM SEL 1 to Gnd	0.96	ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	1.3	μa	≤ 20 μa

S/N 001

Date of Test 5-3-72

Tested By H. Tunel

			Limits
5.4.3.4	Current from MEM SEL 2 to Gnd	0.96 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.3 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	0.96 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 3	1.4 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	0.96 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	1.4 μa	≤ 20 μa
5.4.3.5	Current from READ/WRITE to Gnd	0.96 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	8.1 μa	≤ 20 μa
5.4.3.6	Current from ADDRESS 2^0 to Gnd	0.89 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	0.6 μa	≤ 20μa
	Current from ADDRESS 2^1 to Gnd	0.87 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^1	0.4 μa	≤ 20μa
	Current from ADDRESS 2^2 to Gnd	0.89 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^2	0.6 μa	≤ 20μa
	Current from ADDRESS 2^3 to Gnd	0.88 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^3	0.4 μa	≤ 20μa
	Current from ADDRESS 2^4 to Gnd	0.88 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^4	0.6 μa	≤ 20μa

S/N 001 | Date of Test 5-3-72

Tested By H. Fund

			Limits
Current from ADDRESS 2^5 to Gnd	0.89	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	0.6	μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	NA	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	NA	μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^6	1.0	μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	1.0	μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.1	μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.1	μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	0.9	μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	0.9	μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	0.9	μa	≤ 20μa

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P11216B
	SCALE	REVISION X3	SHEET 5

AV-2-B-1991I-100A-3-69 DWG FORMAT

S/N 001

Date of Test 5-3-72

Tested By A. [illegible]

			Limits
Current from DATA IN BIT 1 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	1.0	μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.0	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	0.9	μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	0.9	μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	1.0	μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	0.9	μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	0.9	μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	0.9	μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	0.9	μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	0.9	μa	≤ 20 μa

S/N 001

Date of Test 5-3-72

Tested By H. [illegible]

			Limits
Current from DATA IN BIT 10 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	0.9	µa	≤ 20 µa
Current from DATA IN BIT 11 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	0.9	µa	≤ 20 µa
Current from DATA IN BIT 12 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	0.9	µa	≤ 20 µa
Current from DATA IN BIT 13 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 13	0.9	µa	≤ 20 µa
Current from DATA IN BIT 14 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	0.9	µa	≤ 20 µa
Current from DATA IN BIT 15 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	1.2	µa	≤ 20 µa
Current from DATA IN BIT 16 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 16	1.2	µa	≤ 20 µa
Current from DATA IN BIT 17 to Gnd	1.1	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	1.2	µa	≤ 20 µa

S/N 001

Date of Test 5-3-72

Tested By H. Freund

			Limit
5.4.4	Verification of open collector on output signals		
5.4.4.3	READ COMPLETE voltage	< 100 mv	≤100 mv
5.4.4.4	DATA OUT BIT 0 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 1 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 2 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 3 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 4 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 5 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 6 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 7 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 8 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 9 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 10 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 11 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 12 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 13 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 14 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 15 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 16 voltage	< 100 mv	≤100 mv
	DATA OUT BIT 17 voltage	< 100 mv	≤100 mv

S/N 001

Date of Test 5-3-72
Tested By H. Fennell

			Limits
5.4.5	Power Consumption (25°C)		
5.4.5.1	Memory +5v current	16.5 ma	
	Memory +5v power	82.5 mw	
	+5V Voltage	+5.00 Volts	
5.4.5.2	DELETED.		
5.4.5.3	Memory -6.9Vcurrent	1.84 ma	
	Memory -6.9Vpower	12.7 mw	
	-6.9V Voltage	-6.90 Volts	
5.4.5.4	Memory idle total power	95.2 mw	≤ 150 mw
5.4.5.6	Memory +5v current	550 ma	
	Memory +5v power	2750 mw	
5.4.5.7	DELETED.		
5.4.5.8	Memory -6.9Vcurrent	144 ma	
	Memory -6.9V power	994 mw	
	-6.9V Voltage	-6.90 volts	
5.4.5.9	Total active power	3744 mw	≤6000 mw
5.4.6	Read Complete Timing		
5.4.6.6	Delay	295 ns	≤ 500 ns
	Duration	295 ns	250 ns min. 450 ns max.

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
	SCALE	REVISION X3	SHEET 9

AV-2-B-19301-100A-3/69 DWG FORMAT

S/N 001 Date of Test 5-3-72
Tested By H. Lund

5.4.7 System Function Test Limits

5.4.7.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

5.4.7.4 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

5.4.7.11 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

5.4.7.17 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

5.4.8 Random Access Capability

5.4.8.7 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

5.4.8.8 Did an error occur?

a) No ✓

Yes _____ Address _____ Bits _____ 0 errors

S/N 001 Date of Test 5-3-72

Tested By [illegible signature]

Limits

b) No ✓

Yes ____ Address ____ Bits ____ 0 errors

c) No ✓

Yes ____ Address ____ Bits ____ 0 errors

5.4.9 Non-Volatility Test

5.4.9.8 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

5.4.10 Memory Select Test

5.4.10.3	Address		0000 (Octal)	0000
5.4.10.4	Address	0001	0000 (Octal)	0000
		0010	0000 (Octal)	0000
		0011	0000 (Octal)	0000
		0100	0000 (Octal)	0000
		0101	0000 (Octal)	0000
		0110	0000 (Octal)	0000
		0111	0000 (Octal)	0000
		1000	0000 (Octal)	0000
		1001	0000 (Octal)	0000
		1010	0000 (Octal)	0000

S/N 001

Date of Test 5-3-72

Tested By H. Lenard

			Limits
Address 1011	0000	(Octal)	0000
1100	0000	(Octal)	0000
1101	0000	(Octal)	0000
1110	0000	(Octal)	0000

5.4.10.6 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

5.4.11 Worst Case Pattern Test

5.4.11.2 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

5.4.11.3 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

S/N 001

Date of Test 5-3-72

Tested By H. Leuel

Limits

5.4.11.4 a) Did an error occur?

No ✓ ______

Yes ______ Address ______ Bit ______ 0 errors

b) Did an error occur?

No ✓ ______

Yes ______ Address ______ Bit ______ 0 errors

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B	
	SCALE		REVISION X2	SHEET 13

AV 2 R 1091 100A 3 (9) DWG FORMAT

S/N ____________ Date of Test ____________
Tested By ____________

Limits

6.2 THERMAL CYCLE

6.2.2 High Temperature

Thermal Resistance

50 minutes _____ K ohms

60 minutes _____ K ohms % change _______

70 minutes _____ K ohms % change _______

80 minutes _____ K ohms % change _______

90 minutes _____ K ohms % change _______

6.2.2.1 +5V current ___ ma

-6.9V current _____ ma Total power ___ mw ≤150 mw

+5V Voltage _____

-6.9 V Voltage _______

6.2.2.2 Did an error occur?

No _______

Yes _______ Address _______ Bit _______ errors

6.2.2.3 -6.9V voltage ___ volts +5V current _______ ma
+5.0V voltage ___ volts
-6.5V current ____ ma Total Power _______ mw ≤6000 mw

6.2.2.4 WC a) Did an error occur?

No _______

Yes _______ Address _______ Bits _______

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11216B
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S/N ____________________ Date of Test ____________

Tested By ____________

WC b) Did an error occur?

No ______

Yes _____ Address _______ Bits __________

WC c) Did an error occur?

No ______

Yes _____ Address _______ Bits __________

WC d) Did an error occur?

No ______

Yes _____ Address _______ Bits __________

6.2.2.5 Did an error occur?

No ______

Yes _____ Address _______ Bits __________

6.2.3 Low Temperature

Thermal Resistance

150 minutes ____________ K ohms

160 minutes ____________ K ohms % change __________

170 minutes ____________ K ohms % change __________

180 minutes ____________ K ohms % change __________

190 minutes ____________ K ohms % change __________

6.2.3.1 Did an error occur?

No ______

Yes _____ Address _______ Bits __________

S/N ______________ Date of Test ______________

Tested By ______________

						Limits
6.2.3.2			+5V current	______	ma	Power Supply
	-6.9V current	_____ ma	Total power	______	mw	$\leq$150 mw
			+5V Voltage	______		
	-6.9V voltage	______				
6.2.3.3			+5V current	______	ma	
	-6.9V current	_____ ma	Total power	______	mw	$\leq$6000 mw

6.2.3.4 Did an error occur?

No ________

Yes ________ Address __________ Bits __________

6.2.3.5 WC a) Did an error occur?

No ________

Yes ________ Address __________ Bits __________

WC b) Did an error occur?

No ________

Yes ________ Address __________ Bits __________

S/N ____________________

Date of Test __________

Tested By ____________

WC c) Did an error occur?

No _______

Yes _______ Address __________ Bits ________

WC d) Did an error occur?

No ________

Yes _______ Address __________ Bits ___________

APPENDIX II

QUALIFICATION TEST PROCEDURES

APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	INITIAL RELEASE	12/23/70	[illegible]
X2	ADDED ±3DB TOLERANCE TO PARA. 7.2 (RANDOM VIBRATION	4-22-71	KHC
X3	Deleted references to +15V. Changed No. of shock directions from six to three as defined in Equipment Spec.	1-16-72	HRT
X4	Changed vacuum limitation 10^{-6} mm Hg to 10^{-5} mm Hg. Changed -6.5V to -6.9V. Incorporated procedural corrections.	4-17-72	HRT

REV STATUS OF SHEETS	REV	X4	X4	X4	X4	X4	X4	X4	X4	X4	X4	X4	X1	X3
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY Bob Lott 12/15/70

CHK BY L. Reynolds 12/23/70

MFG

PROJ NO. 3917

CONTR NO. NAS5-20155

RELEASE NOTICE

APPROVED L Brown DATE 12/23/70

APPROVED [illegible] DATE 12/30/70

MOTOROLA INC. Government Electronics Division

8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

QUALIFICATION TEST PROCEDURE LOW POWER RANDOM ACCESS SPACECRAFT MEMORY

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13675B

SCALE

SHEET 1 OF 13

B-199H-100A-3/69 DWG FORMAT

1.0 SCOPE

This Qualification Test Procedure and Qualification Test Procedure Data Sheet (12-P13676B) define the qualification test requirements for the Low Power Random Access Spacecraft Memory (LP-RASM) Motorola part No. 01-P13666B, Manufactured for NASA, GSFC under contract No. NAS5-20155.

2.0 REFERENCE INFORMATION

2.1 APPLICABLE DOCUMENTS

Document No.	Title
S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13666B	Acceptance Test Procedure Low Power Random Access Spacecraft Memory
12-P11216B	Acceptance Test Procedure Data Sheet Low Power Random Access Spacecraft Memory
12-P13676B	Qualification Test Procedure Data Sheet Low Power Random Access Spacecraft Memory

2.2 The order in which tests are performed (i.e. vacuum, vibration, and shock) may be modified as necessary, depending on availability of test facilities.

3.0 TEST EQUIPMENT AND ENVIRONMENTAL TEST EQUIPMENT

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

ITEM	MANUFACTURER	MANUFACTURER'S MODEL OR TYPE	RANGE & ACCURACY
Oscilloscope	Tektronix	585	50ns/cm
Scope Plug-In	Tektronix	82	Tr = 1.5 ms
Digital Voltmeter	Hewlett-Packard	3440A	Accuracy ±.05% of reading
Counter	CMC	727BN	0.1% ± 1/2 LSB
DC Multifunction Unit	Hewlett-Packard	3444A	0-999.9 ma. 0-9.999 megohms
Pulse Generator	EH	139B	10 Hz to 50 MHz
Power Supplies	Precision Design Inc.	5015-S	0-50V, 1.5 amp.
Power Supplies	Precision Design Inc.	5015-A	0-50V, 1.5 amp

NON-STANDARD TEST EQUIPMENT

(No Calibration Required)

Motorola Plated Wire Memory Tester 01-P11170B001

NOTE: The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE: The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull up resistor to signals coming back from the memory.

Vibration Test Fixture

3.2 ENVIRONMENTAL TEST EQUIPMENT

(Furnished by Motorola environment facility)

The following test equipment or it's equivalent will be needed to perform this test.

ITEM	MANUFACTURER	MODEL NO.
Vibration Tester	LING	275
Vacuum Chamber	NRC	2707
Shock Tester	MRL	2424

4.0 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions:

4.1 POWER SUPPLY VOLTAGE

The unit specified to be tested shall operate from the following DC source voltages, +5V ± 5%, -6.9V ± 5%.

4.2 AMBIENT TEMPERATURE

The unit shall be tested in a laboratory area having temperature of 25 ± 10°C (77 ± 18°F).

4.3 AMBIENT HUMIDITY

Normal laboratory ambient, not to exceed 90%.

4.4 AMBIENT ATMOSPHERIC PRESSURE

Normal laboratory ambient.

4.5 SHIELDING AND ISOLATION REQUIREMENTS

No special precautions are required.

4.6 STABILIZATION PERIOD

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4.7 COOLING

None required.

5.0 PRE-QUAL TESTS

The Pre-Qual Tests are intended to determine correct operation of the LP RASM before proceeding with the Qualification Tests.

The Acceptance Test performed on the LP RASM at the end of the manufacturing phase will suffice for the Pre-Qual Test.

5.1 TEST LOG

This test log shall be used to record the history of the memory starting from the first system test. It shall show all testing, rework and idle time of the memory.

6.0 VACUUM TEST

A vacuum and rapid decompression test shall be performed on the LP RASM. The memory shall be operational during these tests.

6.1 PROCEDURE

6.1.1 Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 1.

Turn on power to all memory associated test equipment.

6.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
Tester	
BD1-BD4 (24 Switches)	UP
Tape Reader Power	Light Off
Run-OFF-Rewind Switch	OFF
Tester Power	Light ON
ADDRESS Switches	DOWN
DATA Switches	DOWN
READ/WRITE	READ
WORD LENGTH	24
READ 1/READ 7 Switch	READ 7
ADDRESS PATTERN	SEQ
DATA PATTERN	SEQ
FREQUENCY	EXT
Interface Box	
MEMORY SELECT SWITCHES	All 2.4V
INPUT CURRENT SWITCH	GND

6.1.2 (CONT.)

CONTROL	SETTING
OUTPUT PULLUP RESISTOR	+5V
INITIATE PULSE SWITCH	PULSE
WC2 SWITCH	OFF
WC SWITCH	OFF
MEMORY POWER	OFF

6.1.2.1 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to +5.0 ± 0.1V. Set the memory supplies to approximately +5V and -6V. Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to +5.0 ± 0.1V and -6.9 ± 0.1V. Set the memory power switch to OFF.

6.1.2.2 Using the scope, adjust the Pulse Generator for +3.0 ± 0.1V positive pulses of 450 ± 10 nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to 500 ± 1.0 KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.

6.1.3 Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors in the Qual Test Data Sheet. Procede immediately to paragraph 6.1.4.

6.1.4 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vaccum pump at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors in the Qual Test Data Sheet.

6.1.5 Continue pumping the chamber until the pressure is 10^{-5} mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF, and turning the TESTER POWER OFF. After the chamber has reached 10^{-5} mmHg, test the memory for five minutes as outlined in paragraph 6.1.3, record any errors in the Qual Test Data Sheet. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, and the TESTER POWER OFF and return the memory to one atmosphere pressure.

7.0 VIBRATION TEST

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

7.1 SINE SWEEP TEST

7.1.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 1 and turn on power to all memory associated test equipment.

Perform paragraphs 6.1.2, 6.1.2.1 and 6.1.2.2.

Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 2. (The axis order may be varied for convenience).

7.1.2 Push the STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton. The tester is now testing the LP RASM for bit errors. Perform a sine sweep over the frequency range of 5-2000 Hz at the levels listed below:

FREQUENCY RANGE	TEST LEVEL
5-25 Hz	0.5 in DA
24-110 Hz	15g PEAK
110-2000 Hz	7.5g PEAK

The sweep rate is to be 2 octaves per minute. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.

7.2 RANDOM VIBRATION

Perform the spectral analysis specified in paragraph 7.0. Push the RESET and START buttons and exercise the memory while applying the following random vibration input.

FREQUENCY RANGE	TEST LEVEL	TOLERANCE
15 Hz	.01 g^2/Hz	$\pm$3db
15-70 Hz	LINEAR INCREASE	Log-Log Plot
70-100 Hz	.31 g^2/ Hz	$\pm$3db

7.2 Cont.

FREQUENCY RANGE	TEST LEVEL	TOLERANCE
100-400 Hz	LINEAR DECREASE	Log-Log Plot
400-2000 Hz	.02 g^2/Hz	±3db

The test time is to be 2 minutes per axis.

Record any errors in the Qual Test Data Record.

Push the STOP button.

7.3 Repeat paragraph 7.1.2 and 7.2, in the two other mutually perpendicular axes as shown in Figure 2. Push the STOP pushbutton. Turn the MEMORY POWER OFF, and then turn the TESTER POWER OFF.

8.0 SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

8.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 1 and apply power to all memory associated test equipment. Set the controls as shown in para. 6.1.2 and perform para. 6.1.2.1 and 6.1.2.2). Mount the LP RASM on the shock table so as to apply the shock in the vertical (Y) axis as shown in Figure 3. (The axes order may be varied for convenience).

8.1.1 Push the STOP and RESET pushbuttons. Turn the MEMORY POWER ON, and push the START pushbutton. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.

8.1.2 Push the RESET and START buttons.
Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors in the Qual Test Data Sheet.

8.1.3 Repeat para. 8.1.1 & 8.1.2 for each of the other two directions as shown in Figure 3. Push the STOP pushbutton. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

9.0 POST QUAL TESTS

To insure that the memory is still operating properly, perform the tests outlined in the acceptance test procedure for the Low Power Random Access Spacecraft Memory, 12-P11215B, with the exception of Section 6.0, TEMPERATURE TESTS. This concludes the Qualification Testing.

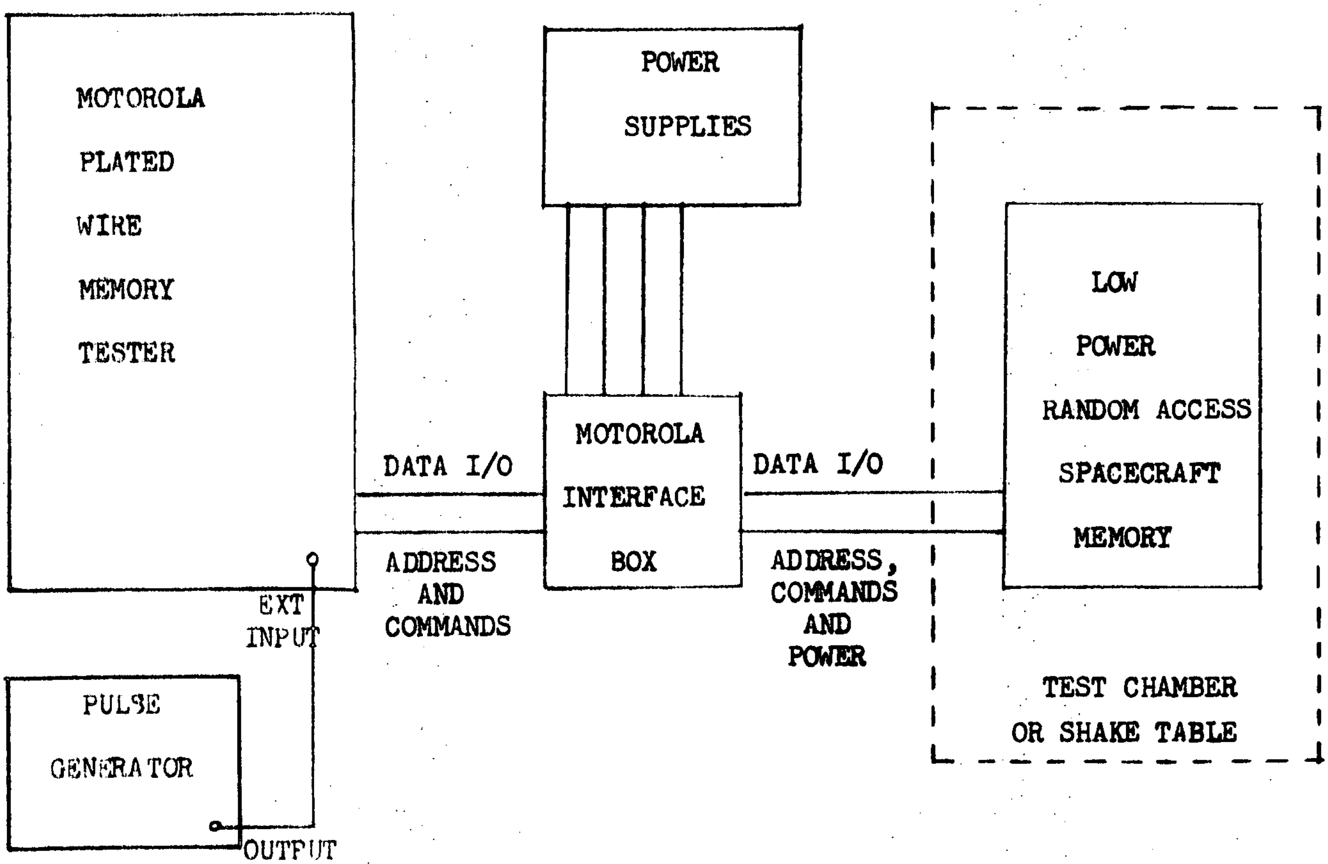

FIGURE 1. TEST SET UP

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13675B
	SCALE	REVISION X4	SHEET 11

AV-2-B-199H-100A-3/69 DWG FORMAT

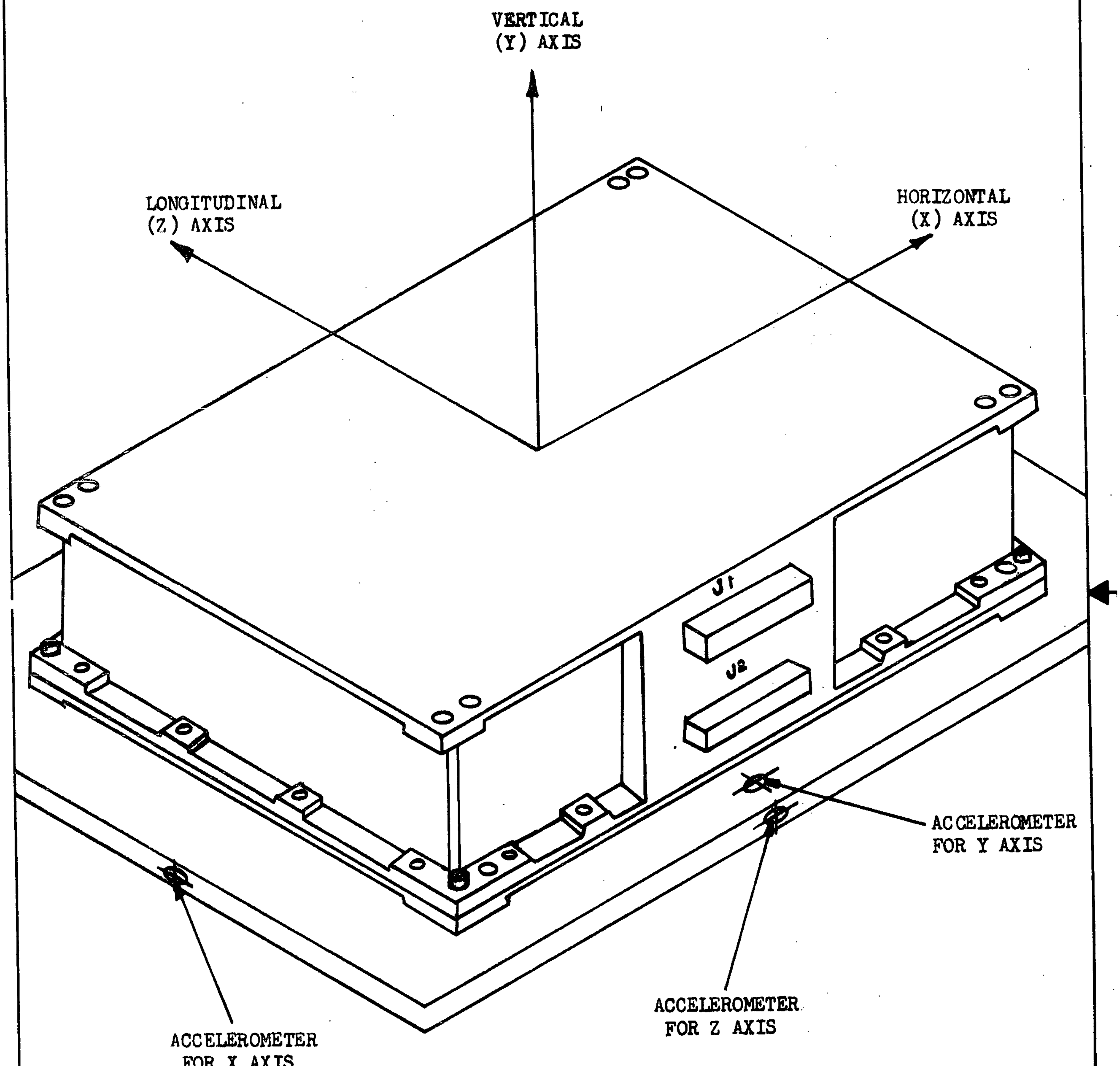

FIGURE 2. VIBRATION AXES

MOTOROLA INC. *Government Electronics Division* 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13675B	
	SCALE *NONE*	REVISION X1		SHEET 12

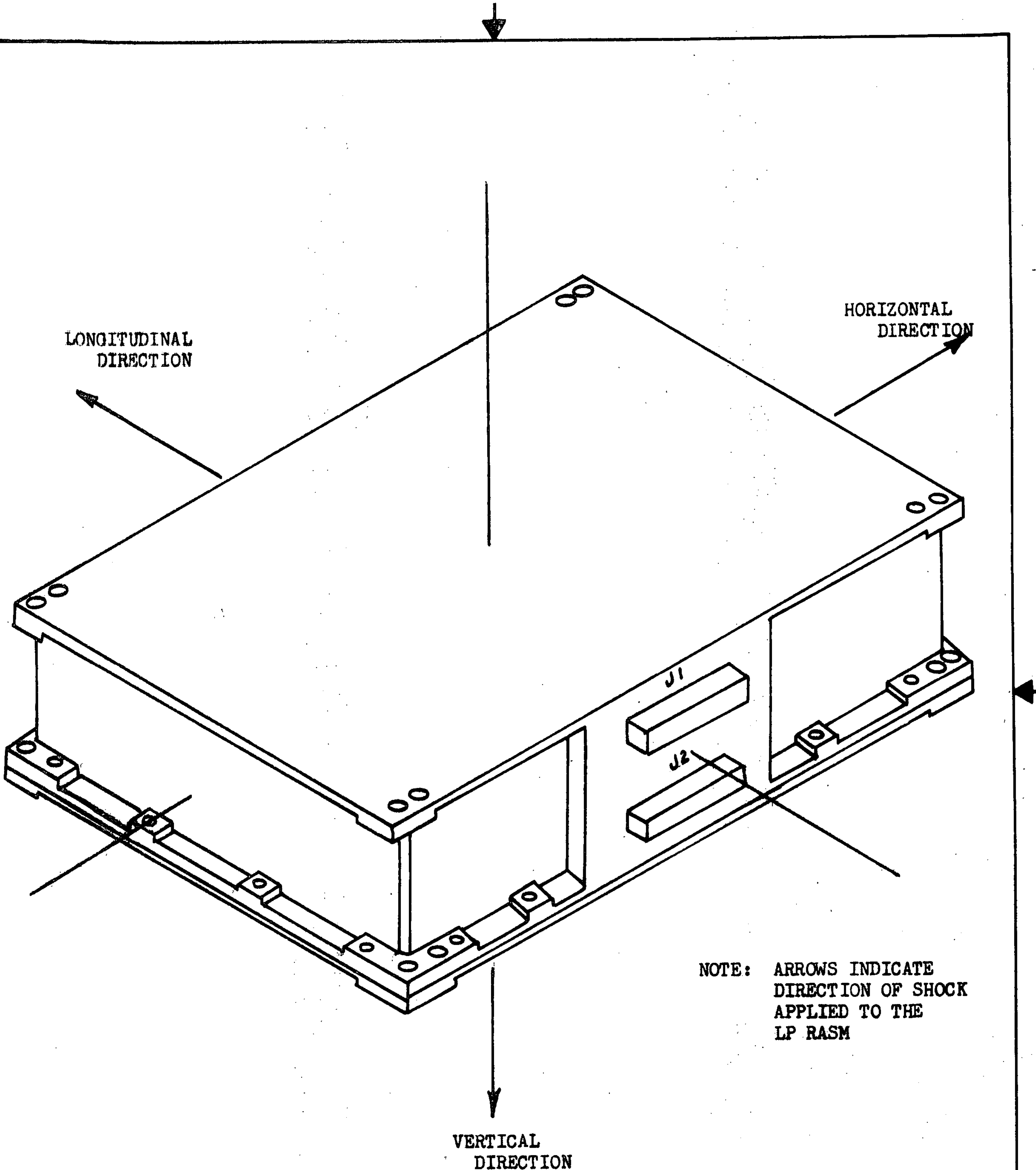

FIGURE 3. SHOCK DIRECTIONS

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13675B
	SCALE NONE	REVISION X3	SHEET 13

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AV 2 B 1 H 1004-3/69 DWG FORMAT

NEXT ASSEMBLY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		X1	INITIAL RELEASE	12/23/70	[illegible]
		X2	Changed No. at shock directions from six to three. Added sheet for Test Data and notes.	1-16-72	HRT
		X3	Added sheet 6.	2-22-72	HRT

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THIS DATA RECORD CONTAINS THE FOLLOWING SHEETS:
(REFER TO SHEET 2, PARAGRAPH 3.0).

1	13
2	14
3	15
4A, 4B, 4C	16
5A, 5B	17
6	18
7	19
8	
9	
10	
11	
12	

REV STATUS OF SHEETS							
	REV	X2	X2	X2	X2	X2	X3
	SHEET	1	2	3	4	5	6

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY Bob Lott 12/5/70

CHK BY [illegible] 12/../70

MFG

PROJ NO. 3917

CONTR NO. NAS5-20155

RELEASE NOTICE

APPROVED [illegible] DATE 12/23/70

APPROVED [illegible] DATE 12/../70

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

QUALIFICATION TEST PROCEDURE DATA SHEET
LOW POWER RANDOM ACCESS SPACECRAFT MEMORY

SIZE A | CODE IDENT NO. 94990 | DWG. NO. 12-P13676B

SCALE | SHEET 1 OF ~~4~~ 19

AV-1-B-199H-100A-3/69 DWG FORMAT

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C.3

1.0 SCOPE

This qual test data sheet is to be used to record the data called out in the qualification test procedure Low Power Random Access Spacecraft Memory 12-P13675B.

2.0 REFERENCE INFORMATION

2.1 APPLICABLE DOCUMENTS

DOCUMENT NO.	TITLE
S-562-P-24	Low Power Random Access Spacecraft Memory.
12-P13675B	Qualification Test Procedure Low Power Random Access Spacecraft Memory.

2.2 TEST LIMITS

In all tests the test limit is no bit errors.

3.0 TEST DATA & NOTES

Sheet 4A reflects only data from the failed vibration test performed 4-20-72.
H. Lund

Vibration data on sheets 4B and 5A reflects test failed on 4-26-72.

H. Lund

Vibration data on sheets 4C and 5B reflects test passed on 4-29-72.

H. Lund

Sheets 7 through 19 are records of environmental test set-ups and conditions. These sheets contain no Memory Unit Test Data. H. Lund

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X2	SHEET 2

AV-2-B-190H-100A-3 69 DWG FORMAT

6.0 VACUUM TESTS

6.1.3 Did Any Bit Errors Occur?

No ✓

Yes ______ Address ______ Bits ______

6.1.4 Fast Decompression

Date 4-25-72 Tested By H. Sewell

Did Any Bit Errors Occur?

No ✓

Yes ______ Address ______ Bits ______

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X2	SHEET 3

6.1.5 Hard Vacuum

Date ~~4-2?-72~~ HRT   Tested By ~~H. Tanaed~~ HRT

Did Any Bit Errors Occur?

No ~~✓~~ HRT   See Next Sheet

Yes ______   Address ______ Bits ______

7.0 VIBRATION

Date 4-20-72   Tested By H. Tanaed

7.1.2 Sine Sweep

Axis X - Did Any Bit Errors Occur?

No ______

Yes ______ Freq ______ Address ______ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ______

Yes ______ Freq ______ Address ______ Bits ______

Axis Z - Did Any Bit Errors Occur?

No ______

Yes ✓ Freq ≈ 10 cps Address numerous Bits numerous

7.2. and 7.3 Random Vibration

Axis X - Did Any Bit Errors Occur?

No ______

Yes ______ Freq ______ Address ______ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ______

Yes ______ Freq ______ Address ______ Bits ______

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85257	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P136760
	SCALE	REVISION	SHEET A

AV-7-B 1500-16A-3/69 DWG FORMAT

6.1.5 Hard Vacuum

Date 4-25-72 Tested By H. Leuned

Did Any Bit Errors Occur?

No ✓

Yes ______ Address ______ Bits ______

7.0 VIBRATION

Date 4-26-72 Tested By H. Leuned

7.1.2 Sine Sweep

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ______ Freq ______ Address ______ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ______ Freq ______ Address ______ Bits ______

Axis Z - Did Any Bit Errors Occur?

No ______

Yes ______ Freq ______ Address ______ Bits ______

7.2. and 7.3 Random Vibration

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ______ Freq ______ Address ______ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ______ Freq ______ Address ______ Bits ______

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X2	SHEET 4B

AV-2-B-199H-100A-3/69 DWG FORMAT

6.1.5 Hard Vacuum

Date ____________ Tested By ____________

Did Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits ______

7.0 VIBRATION

Date 4-29-72 Tested By Larry L Brown

7.1.2 Sine Sweep

Axis X - Did Any Bit Errors Occur?

No ✓ LB 4/29/72

Yes ________ Freq ________ Address ________ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ✓ LB 4/29/72

Yes ________ Freq ________ Address ________ Bits ______

Axis Z - Did Any Bit Errors Occur?

No ✓ LB 4/29/72

Yes ________ Freq ________ Address ________ Bits ______

7.2 and 7.3 Random Vibration

LB 4/29/72

Axis X - Did Any Bit Errors Occur? * Test Run twice, First time a single random error occured (could have been noise induced). 2nd time No errors.

No ✓ *

Yes ________ Freq ________ Address ________ Bits ______

Axis Y - Did Any Bit Errors Occur?

No ✓ LB 4/29/72

Yes ________ Freq ________ Address ________ Bits ______

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X2	SHEET 4C

AV-2-B-19911-100A-3/69 DWG FORMAT

TBT FAILED

7.2 and 7.3 Cont.

Axis Z - Did Any Bit Errors Occur?

No ________

Yes ✓ Freq NA Address Numerous Bits Numerous

8.0 SHOCK TEST

Date 5-2-72 Tested By H. Leuerd

8.1.1 6 Millisecond Duration Shock

Y Direction - Did Any Bit Errors Occur?

No ✓ H. Leuerd

Yes ________ Address ________ Bits ________

Z Direction - Did Any Bit Errors Occur?

No ✓ H. Leuerd

Yes ________ Address ________ Bits ________

X Direction - Any Bit Errors Occur?

No ✓ H. Leuerd

Yes ________ Address ________ Bits ________

8.1.2 and 8.1.3 12 Millisecond Duration Shock

Y Direction - Did Any Bit Errors Occur?

No ✓ H. Leuerd

Yes ________ Address ________ Bits ________

Z Direction - Did Any Bit Errors Occur?

No ✓ H. Leuerd

Yes ________ Address ________ Bits ________

MOTOROLA INC. Government Electronics Division 8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X2	SHEET 5A

AV-2-B-1991-100A-3 69 DWG FORMAT

7.2 and 7.3 Cont.

Axis Z - Did Any Bit Errors Occur?

No ✓ LB 4/29/72

Yes ________ Freq ______ Address _______ Bits ________

8.0 SHOCK TEST

Date ________ Tested By __________________

8.1.1 6 Millisecond Duration Shock

Y Direction - Did Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits _________

Z Direction - Did Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits _________

X Direction - Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits _________

8.1.2 and 8.1.3 12 Millisecond Duration Shock

Y Direction - Did Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits _________

Z Direction - Did Any Bit Errors Occur?

No ____________

Yes ____________ Address ________ Bits _________

8.1.2 and 8.1.3 Cont.

X Direction - Did Any Bit Errors Occur?

No ✓

Yes ______ H. [illegible] Address ______ Bits ______

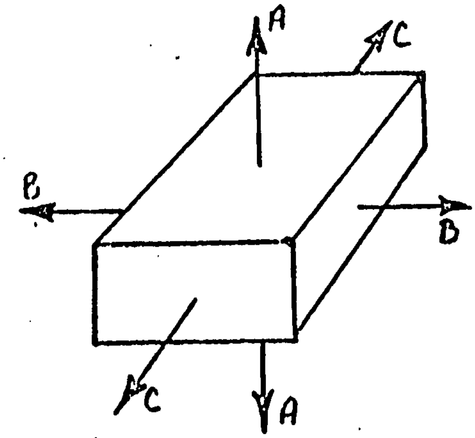
5-2-72

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13676B
	SCALE	REVISION X3	SHEET 6

AV-2-B-1991I-100A-3 69 DWG FORMAT

MOTOROLA INC.
Government Electronics Division
Aerospace Center

VIBRATION TEST



Sheet ' of ' Date 4/20/71

Project 3717 Unit MEMORY

Serial No. 001

Operator J Brunsfield

Observer L. GREEN

Cycle Time 17 12 Freq. 5 to 2000 cps. 5 HZ

Drive Monitor
Sig. Gen ____

Accel 13

Reason for test ____

5-25 HZ @ .5DA 24-110 HZ @ 15G 110-2000 HZ @ 7.5G

Axis	Time Start	Time Stop	Total Time		RMS, MV E	RMS G's	Remarks
A	1100	1102	2 sec		34	8.4	SHAPED RANDOM NOISE
A	1020	1020	1 sec		.5	15-7.5 Pk	5-2000-5 HZ

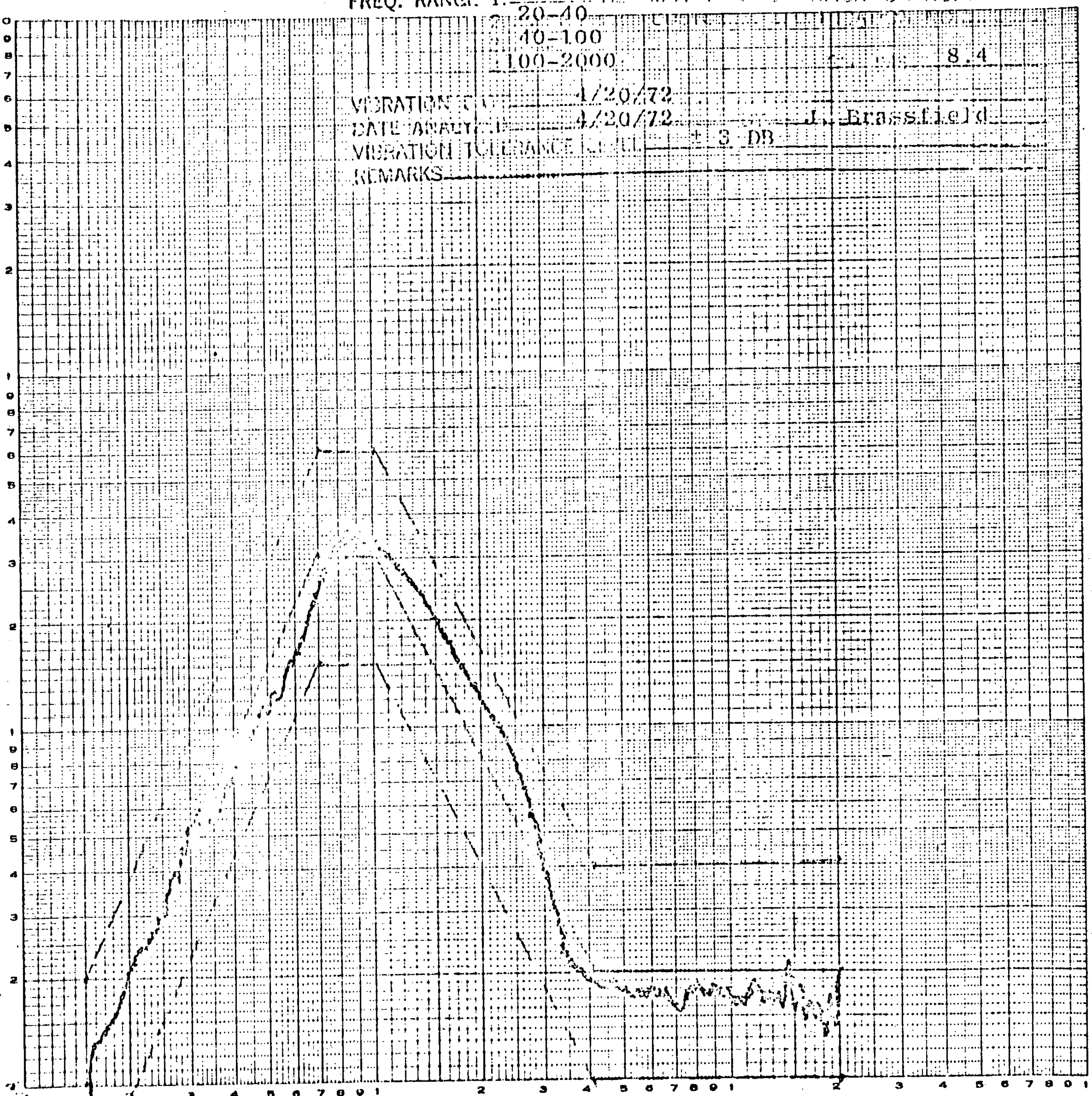
MOTOROLA/GED K0151 1/69

PROJECT ____ UNIT ____ SER. NO. ____

A AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. .125 AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. .25 AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. .50 AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4. 1.25 AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOR SPECIFICATION NO. ____



MOTOROLA INC.
Government Electronics Division
Aerospace Center

VIBRATION TEST

Sheet 1 of 1 Date 1/26

Project 917 Unit MEMORY

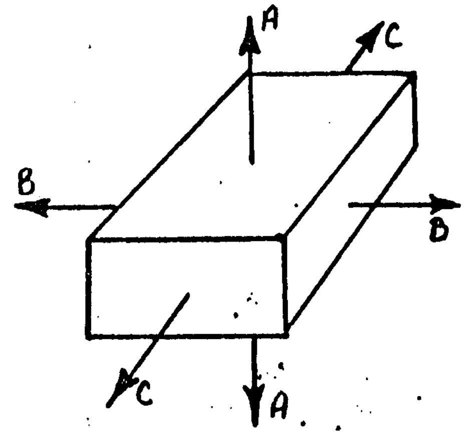
Serial No. 001

Operator J. Burnfield

Observer L. GREEN

Cycle Time 8 16 Freq. 5 to 2000 cps.

Reason for test



Drive Monitor
Sig. Gen

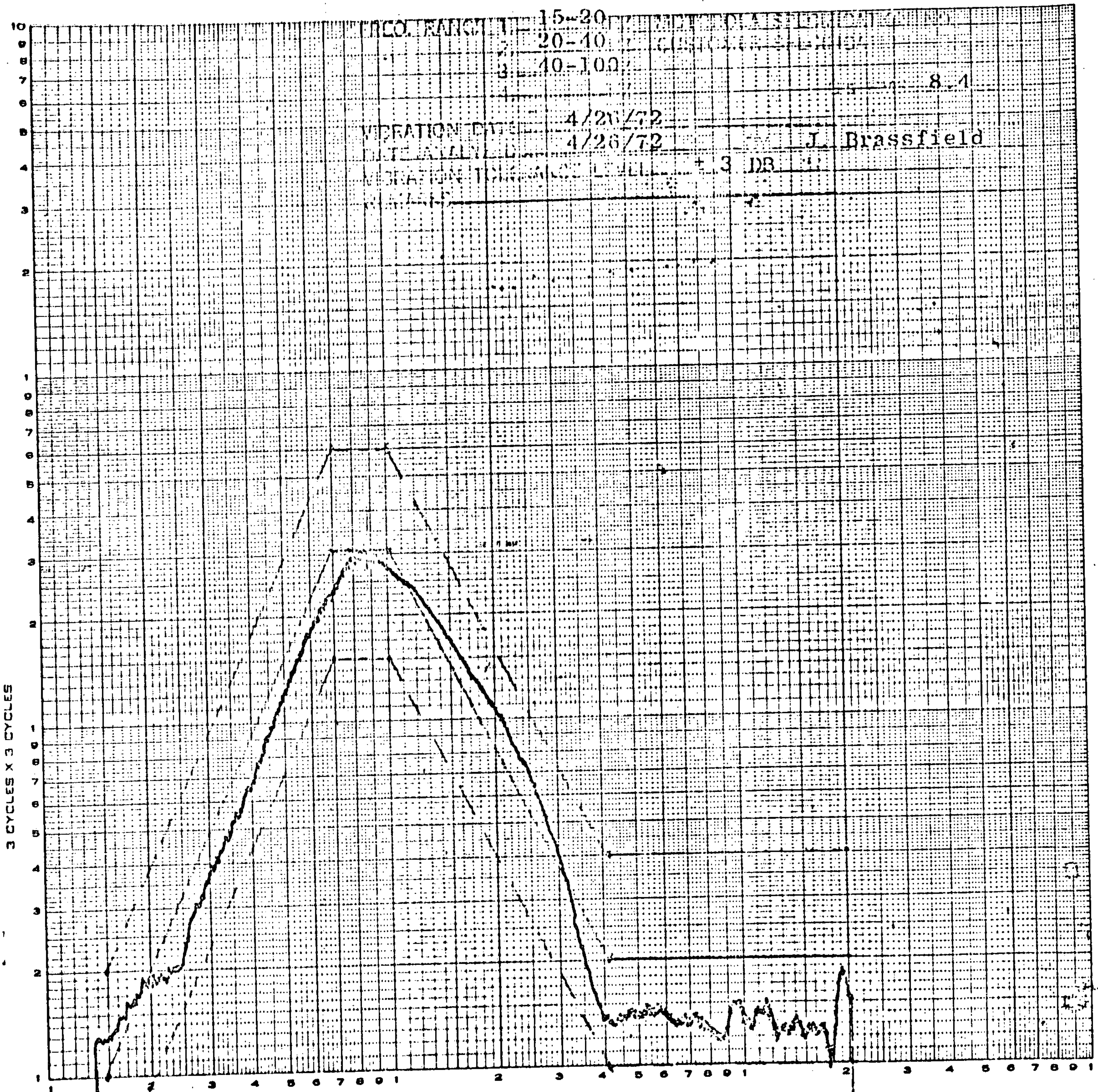
Accel 13

Axis	Time Start	Time Stop	Total Time		E	G	Remarks
A	0830	0947	17 00		.5	15-7.5	5-2000 HZ
A	1000	1002	2 00			8.4 RMS	SHAPED RANDOM
B	1030	1047	17 00		.5	15-7.5	5-2000 HZ
B	1100	1102	2 00			8.4	SHAPED RANDOM NOISE
C	[illegible]	[illegible]	[illegible]			8.4	" " "

PROJECT 3917 UNIT MEMORY SER. NO. 001

A AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. .125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. .25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. .50 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 1. .25 HZ AVG. TIME 4. 10 SECONDS



C

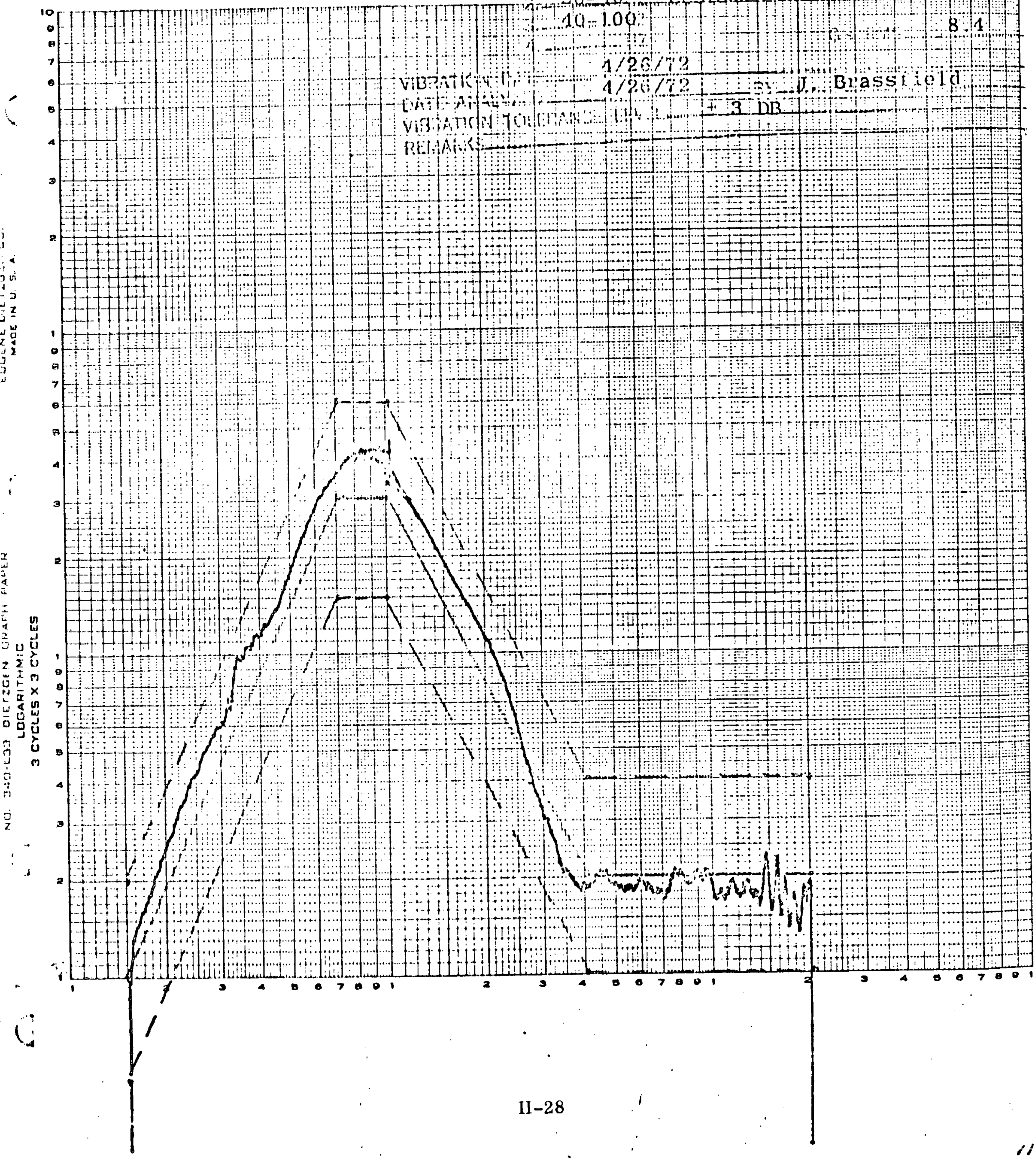
10

PROJECT 5917 UNIT [illegible] SER. NO.

B & C AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. 125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. 25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. 50 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4. 25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1 15-20 HZ MOTOROLA SPECIFICATION NO.
2 20-40 HZ CUSTOMER SPECIFICATION NO.
3 40-100 HZ
4 HZ



K+E AUDIO FREQUENCY 46 6862
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT 3917 UNIT MEMORY SER. NO. 001

B AXIS FREQ. RANGE 5-2000 HZ

PLOTTER CAL. FREQ X Y 10DB/IN.

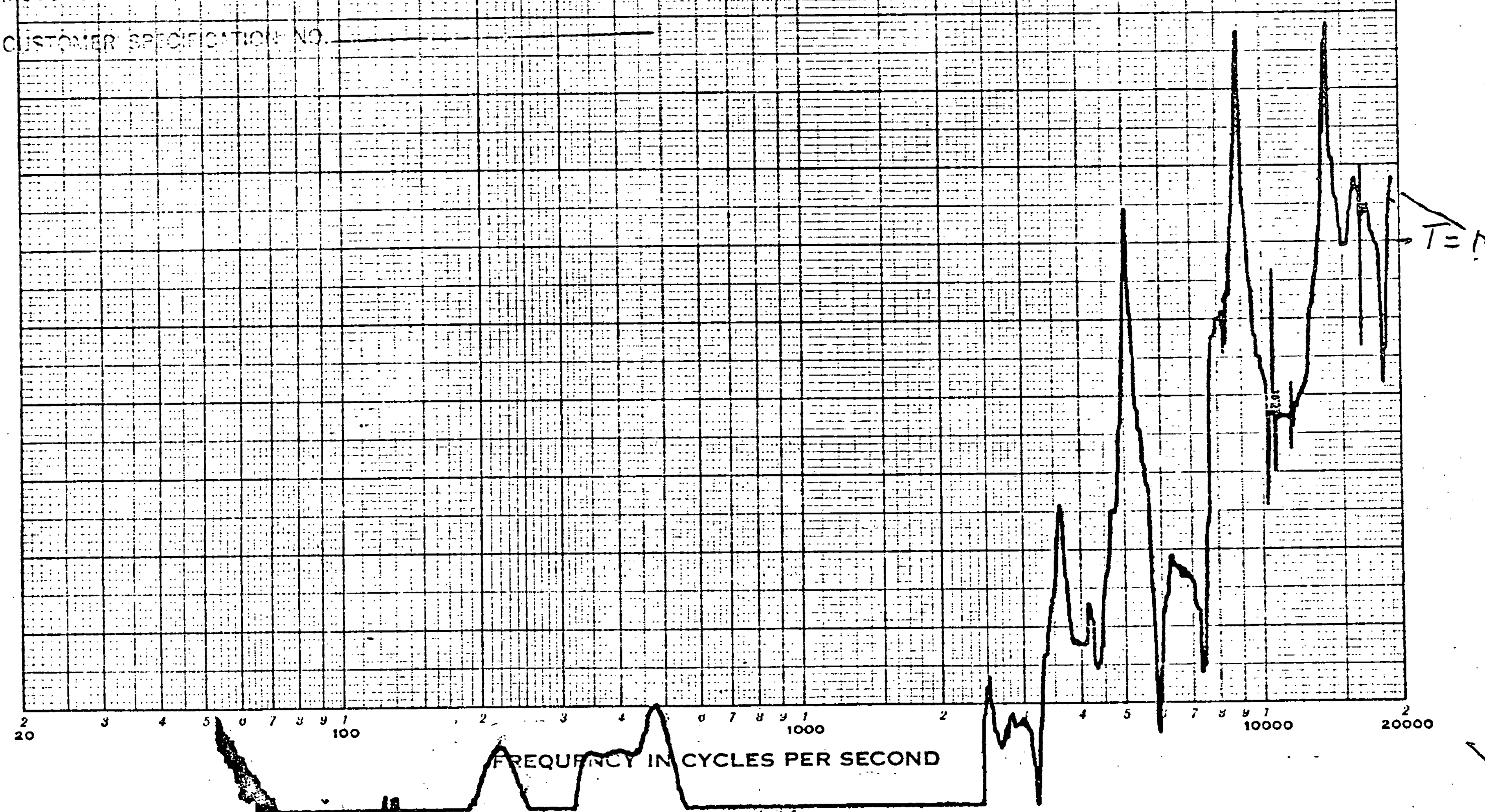
ACCELERATION 7.5 15 PKGS. DISPLACEMENT .5 DA

VIBRATION DATE 4/26/72 BY J. Mansfield

REMARKS Accl. #4 S/W DRIVER

MOTOROLA SPECIFICATION NO. T/F in Plot

CUSTOMER SPECIFICATION NO.



MOTOROLA INC.
Government Electronics Division
Aerospace Center

VIBRATION TEST

Sheet 1 of 1 Date 4-29-72

Project 3917 Unit L.P.R.A.S.M.

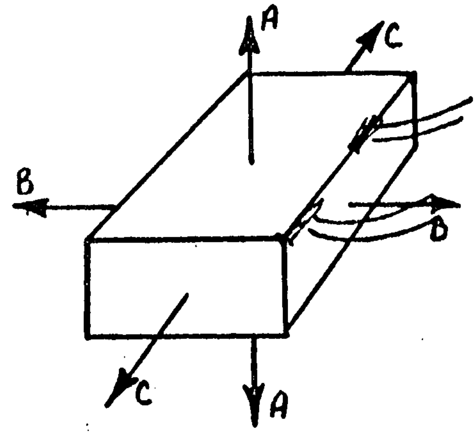
Serial No. 001

Operator O. SMITH

Observer L GREEN

Cycle Time 4^{20} Freq. 5 to 2k cps.

Reason for test



Drive Monitor
Sig. Gen 1 Accel 13

Axis	Time Start	Time Stop	Total Time		/IK EDA	G	Remarks
Z	836	840^{20}	4^{20}		.5	15 & 7.5	5-2KHZ PLOT
Z	953	955	2^{00}			8.4 RMS	SHAPED RANDOM NOISE
X	1004	1006	2^{00}			8.4 RMS	" " "
X	1007	1009	2^{00}			8.4 RMS	" " "
X	1012	1016^{20}	4^{20}		.5	5 & 7.5	5-2KHZ PLOT
Y	1049	1053^{20}	4^{20}		.5	5 & 7.5	5-2KHZ
Y	1116	1120	2^{00}			8.4 RMS	SHAPED RANDOM NOISE

PROJECT 3917 UNIT L.P.R.A.S.M. SER. NO. 001

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. .125Z AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. .25HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. .50 AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 1. .25 AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 10-20
2. 20-40
3. 40-100
4. 100-2K

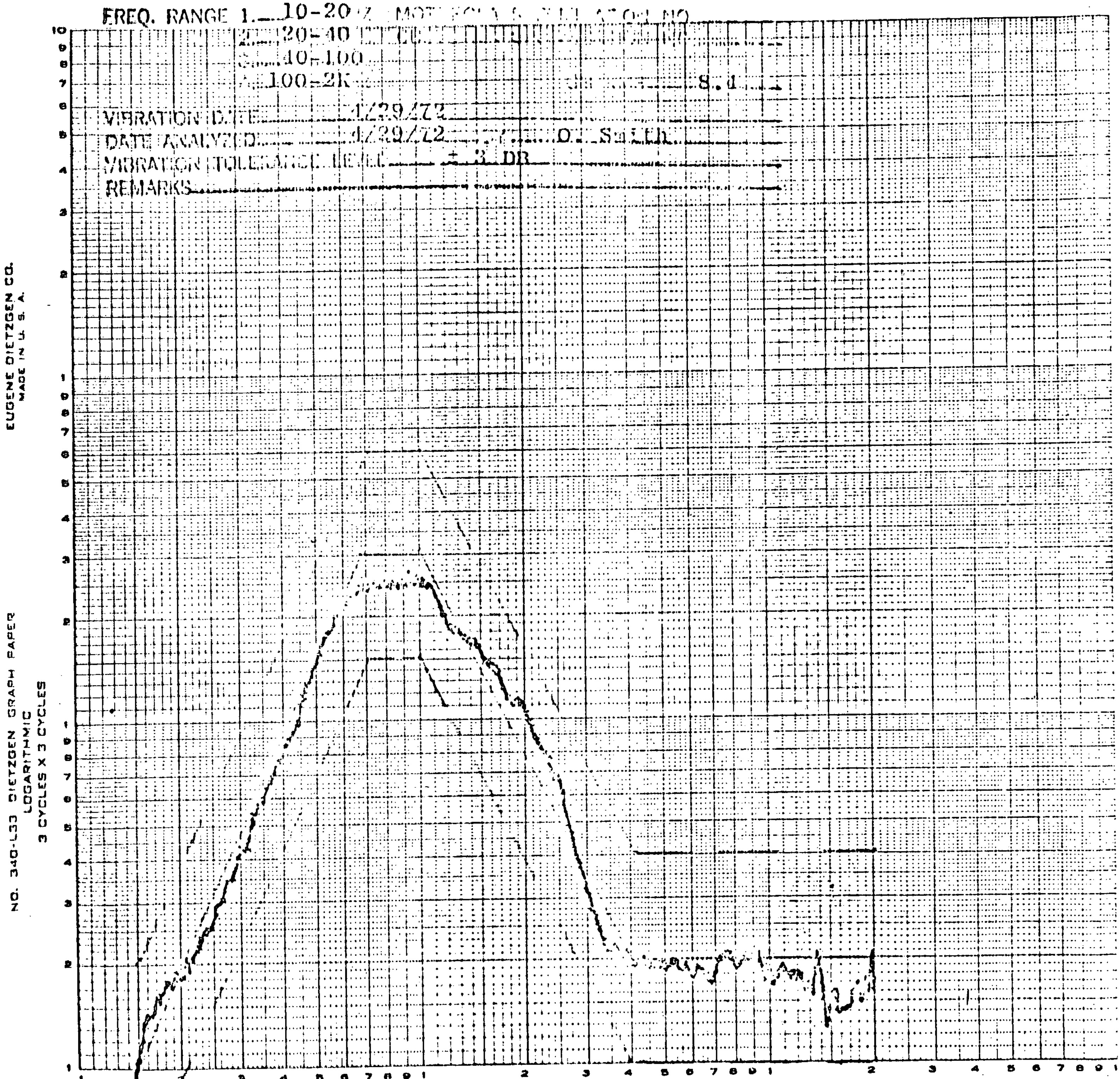
8.1

VIBRATION DATE 4/29/72

DATE ANALYZED 4/29/72 D. Smith

VIBRATION TOLERANCE LEVEL ± 3 DB

REMARKS



14

PROJECT 3917 UNIT L. P. R. A. S. M. SER. NO. --001

X and/or Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

ILTER B.W. 1. 5 HZ SCAN RATE 1. .125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. .25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. .50 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 1.25 HZ AVG. TIME 4. 10 SECONDS

REQ. RANGE 1. 10-20 HZ MOTOROLA SPECIFICATION NO.
20-40 CUSTOMER SPECIFICATION NO.
40-100
100-2K 8.4
BRATION DATE 4/29/72
DATE ANALYZED 4/29/72 BY O. Smith
BRATION TOLERANCE ± 3 DB
MARKS

15

K+E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT 3917 UNIT L.P.R.A.S.M. SER. NO. 001

Z AXIS FREQ. RANGE 5-2KHZ

PLOTTER CAL FREQ X Y 10 DB/IN

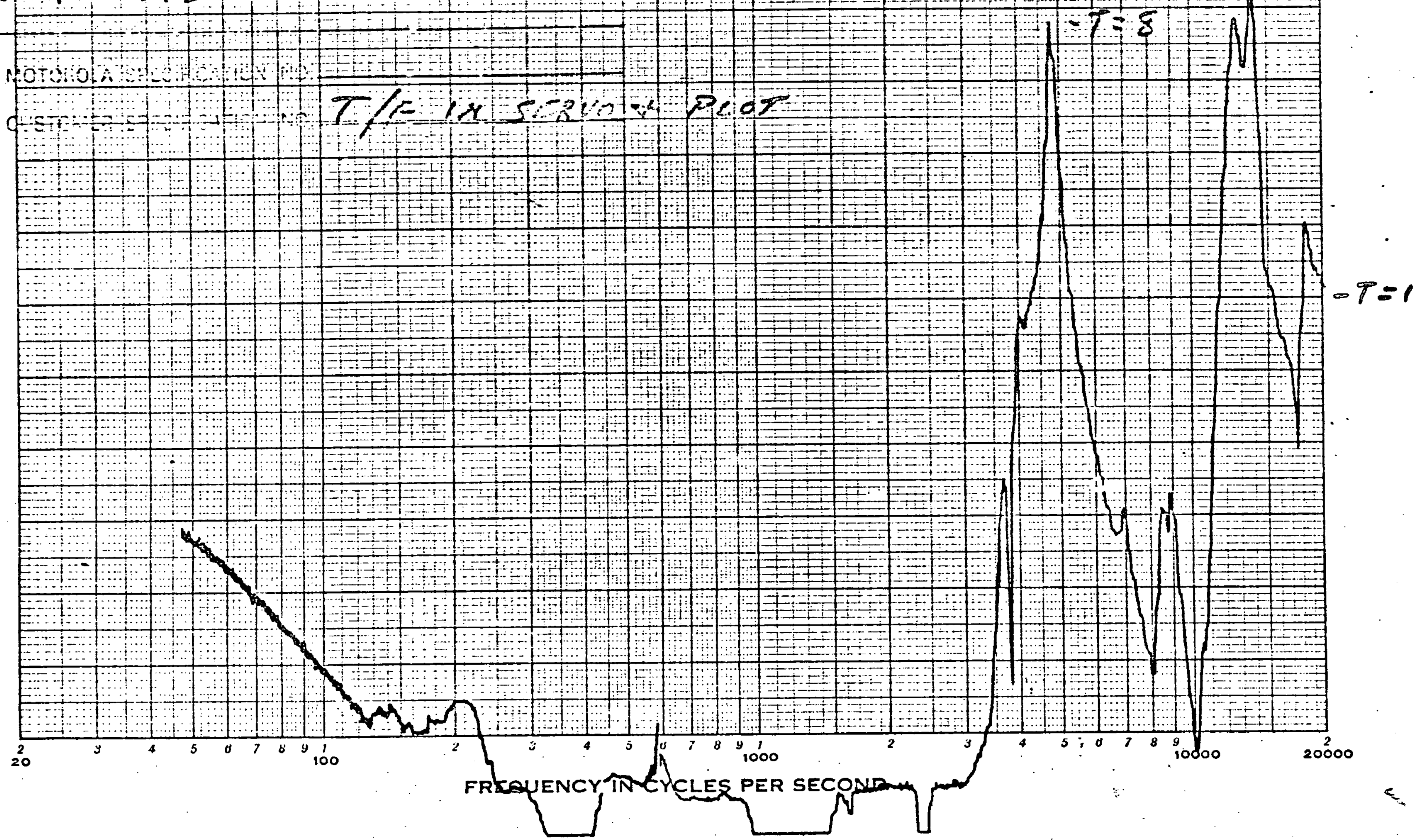
ACCELERATION 15-7 PKGS DISPLACEMENT .5 DA

VIBRATION DATE 4-29-72 BY O. Smith

REMARKS Y AXIS ACCEL VS DRIVER.

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO. T/F IN SERVO PLOT



K+E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT 3917 UNIT L.P.R.A.S.M. SER. NO. 001

X AXIS FREQ. RANGE 5-2KHZ

PLOTTER CAL. FREQ X Y 10DB/IN

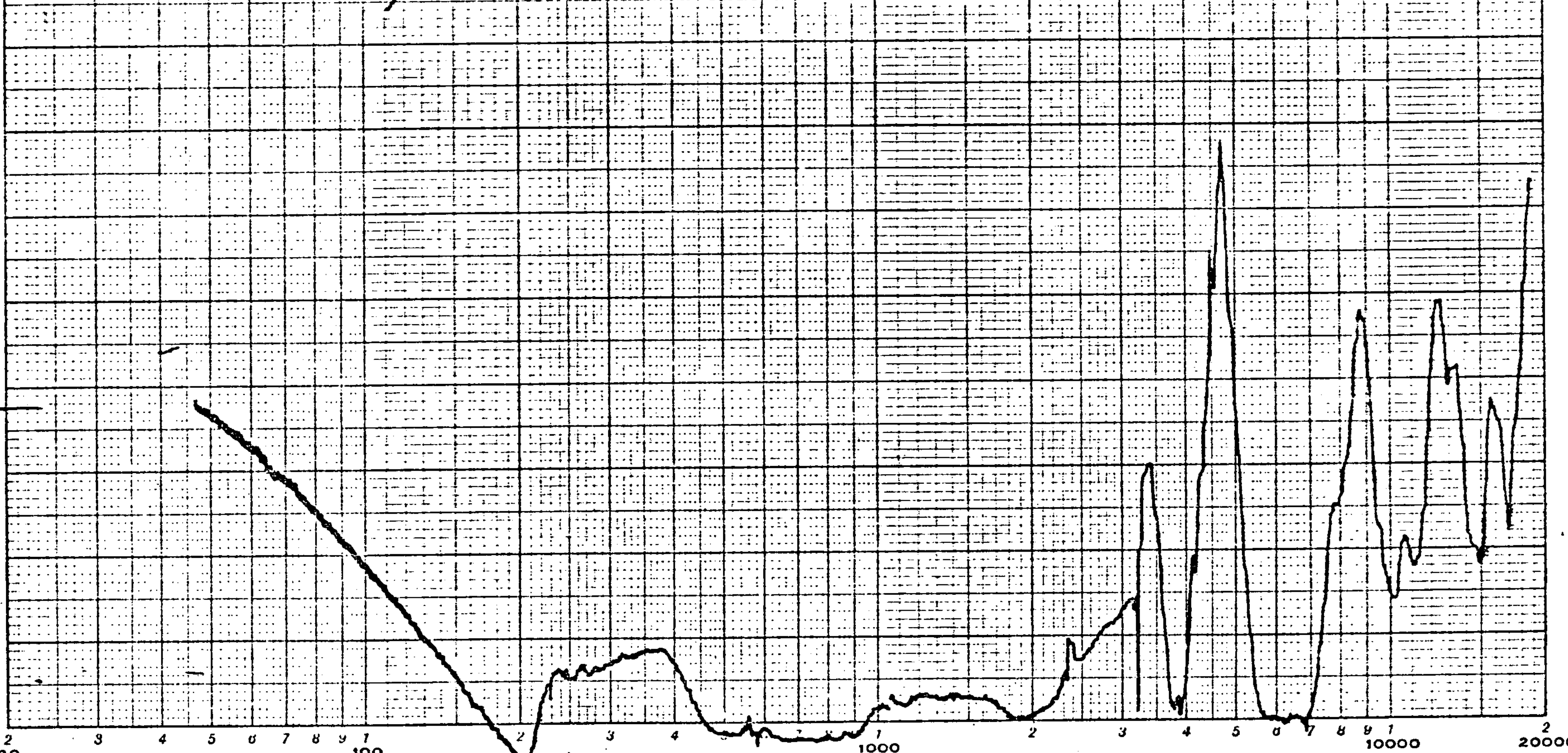
ACCELERATION 15-7 FREQS. DISPLACEMENT .5 DA

VIBRATION DATE 4-29-72 BY O. SMITH

REMARKS X AXIS ACCEL. V.S. DRIVER

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO. T/E IN SERVO + PLOT



II-34

HIGH VACUUM TEST

Unit LP RASM MEMORY	Project 3917
Model 01-P13666B	Specification 12-P13675QTP
Serial 001	Operator ART HAWKINS
Vacuum System No. 3	Observer HERSHEL TWEED

Date 4-25-72

VACUUM ONLY

TIME	PRESSURE (mm Hg A)											REMARKS
0745	AMB											START PUMPING
0755	6.7×10^{-5}											
0830	2.0×10^{-5}											
0900	1.8×10^{-5}											
0930	1.3×10^{-5}											
1000	1.0×10^{-5}											
1030	8.6×10^{-6}											Vent to [illegible]
1032	AMB											BELL JAR OPENED
												END TEST

MOTOROLA
Government Electronics Division
AEROSPACE CENTER
8201 EAST McDOWELL ROAD SCOTTSDALE ARIZONA

SHOCK TEST
(DROP)

Sheet 1 of 1586

Date 5-2-72

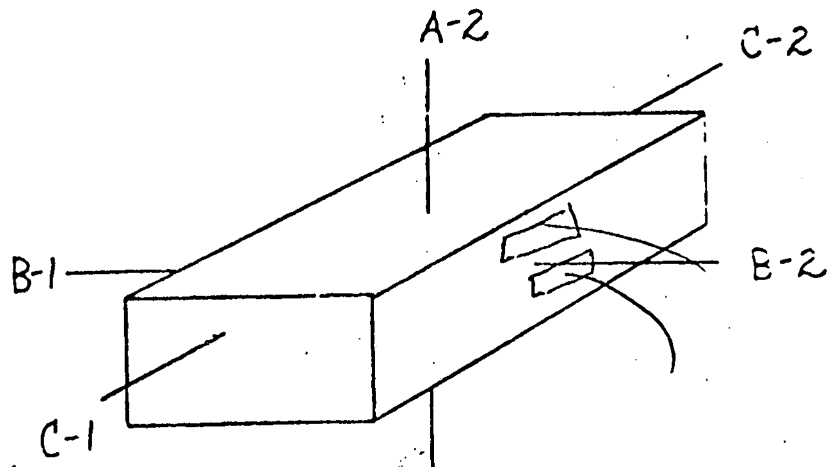
Project 3917

Unit Memory SN-01

Operator Morrison

Observer L. GREEN

Vibration Mounts NONE



No. of drops on each ~~face~~ axis 1 total of 3 at each pulse duration or total of 6 per unit

Acceleration 30 g ½ sine

Duration ~~12~~ 6 & 12 Milliseconds

6 ms. (1–3) 12 ms (5–7)

Axis	Face	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1			/		/															
	2																				
B	1																				
	2	/					/														
C	1		/					/													
	2																				

Remarks $\boxed{6 \text{ ms}}$ 1 ea ½" red green with 2 mech filter pads BFF @ 2K
drop height ≈ 3/4"
$\boxed{12 \text{ ms}}$ 1 ea "1" green closed & 1 ea 1" red open BFF @ 2K
drop height ≈ 3 3/4"

APPENDIX III

ACCEPTANCE TEST PROCEDURES

* APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
X1	INITIAL RELEASE	2-24-72	H. Tweed

ASTERISK INDICATES DATA WHICH IS NONMANDATORY - FOR INFORMATION ONLY.

REV	
SHEET	
REV STATUS OF SHEETS	REV
	SHEET

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE	DR BY H. Tweed	MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252
	CHK BY	
	MFG / PROJ NO. 3917	ACCEPTANCE TEST PROCEDURE FOR PLATED WIRE MEMORY STACK 4K x 18 (1024 WORD LINES, 144 DIGIT LINES) *
MATERIAL:	CONTR NO. NAS5-20155	
	RELEASE NOTICE	
	APPROVED L. Brown DATE 2/24/72	SIZE A / CODE IDENT NO. 94990 / DWG. NO. 12-P11005C
	APPROVED DATE	SCALE / SHEET 1 OF 11

AV-1-C-199H-100A-7/70 DWG FORMAT

1.0 SCOPE

1.1 This test procedure specifies the electrical tests to be performed on all 01-P13660B plated wire memory stacks.

2.0 APPLICABLE DOCUMENTS

2.1 Drawing No. 69-P13667B, Interconnection Diagram.

2.2 Drawing No. 01-P13660B, Memory Stack Assembly.

2.3 Schematic Diagram for Word Drive Test Adapter Box.

3.0 REQUIREMENTS

3.1 TEST EQUIPMENT

3.1.1 Program generator capable of generating the test pattern shown in Figure 5.

3.1.2 Digit current generator capable of generating the digit currents specified in Sections 3.4.2 and 3.4.3 and Figure 3.

3.1.3 Word current generators capable of generating word currents specified in Sections 3.4.2 and 3.4.3 and Figure 3.

3.1.4 Oscilloscope, Tektronix 547 with 1A1 plug-in.

3.1.5 Current probe, Tektronix 6046 with 1A5 plug-in.

3.1.6 Digit line interface board.

3.1.7 Word line interface board.

3.1.8 Word drive test adapter box.

3.2 STACK TESTER/ADAPTER BOX/STACK INTERCONNECT

3.2.1 The interconnections between the EH8500 Stack Tester, the Word Drive Test Adapter Box and the Word Line Interface Board are shown in Figure 1.

3.3 WORD LINE MATRIX AND ADDRESSING

3.3.1 The transistor switch matrix for a memory plane is shown in Figure 2. The address matrix for all word lines in the stack is given in Table 1.

3.4 TEST CONDITIONS

3.4.1 <u>Sense Termination</u>

The sense lines are to be terminated in the Z_o of the sense lines when monitoring output signals ($Z_o = 100 \pm 5$ ohms). The terminating resistors are mounted on the Digit Line Adapter Board.

3.4.2 <u>Current Pulse Waveforms</u>

The current pulse waveforms (as shown in Figure 3) are to be set up initially using a current probe to monitor the word and digit currents at the locations shown in Figure 4. The amplitudes of all currents are given in Figure 3 and Section 3.4.3.

3.4.2.1 The overshoot on any current shall be less than 2% of the specified current amplitude.

3.4.2.2 Pulse to aberrations on any current shall be less than 2% of the specified current amplitude.

3.4.2.3 The droop on any current shall be less than 2% of the specified current amplitude.

3.4.2.4 The overlap of word and digit currents is specified in Figure 3.

3.4.2.5 All times specified are ± 2% or one nanosecond, whichever is greater.

3.4.3 Current Amplitudes

Current amplitudes are in milliamperes ± 1%, as measured at mid-point of the flat top.

3 4.3.1 Read Current = I_{WR} = 490 ma.

3.4.3.1 Write Currents:

Word Current = I_{WW} = 490 ma.

	+25°C	+95°C	-45°C
Digit Current I_{DW1}	42.5	37.0	50.0
Digit Current I_{DW2}	40.5	35.0	47.5

3.4.3.3 Disturb Currents:

Word Current = I_{WD} = 540 ma

	+25°C	+95°C	-45°C
Digit Current I_{DD1}	47.0	41.0	55.5
Digit Current I_{DD2}	49.5	43.0	58.5

3.4.4 Temperature Testing

All electrical tests shall be performed at the three temperatures. The tests shall be run in the following order.

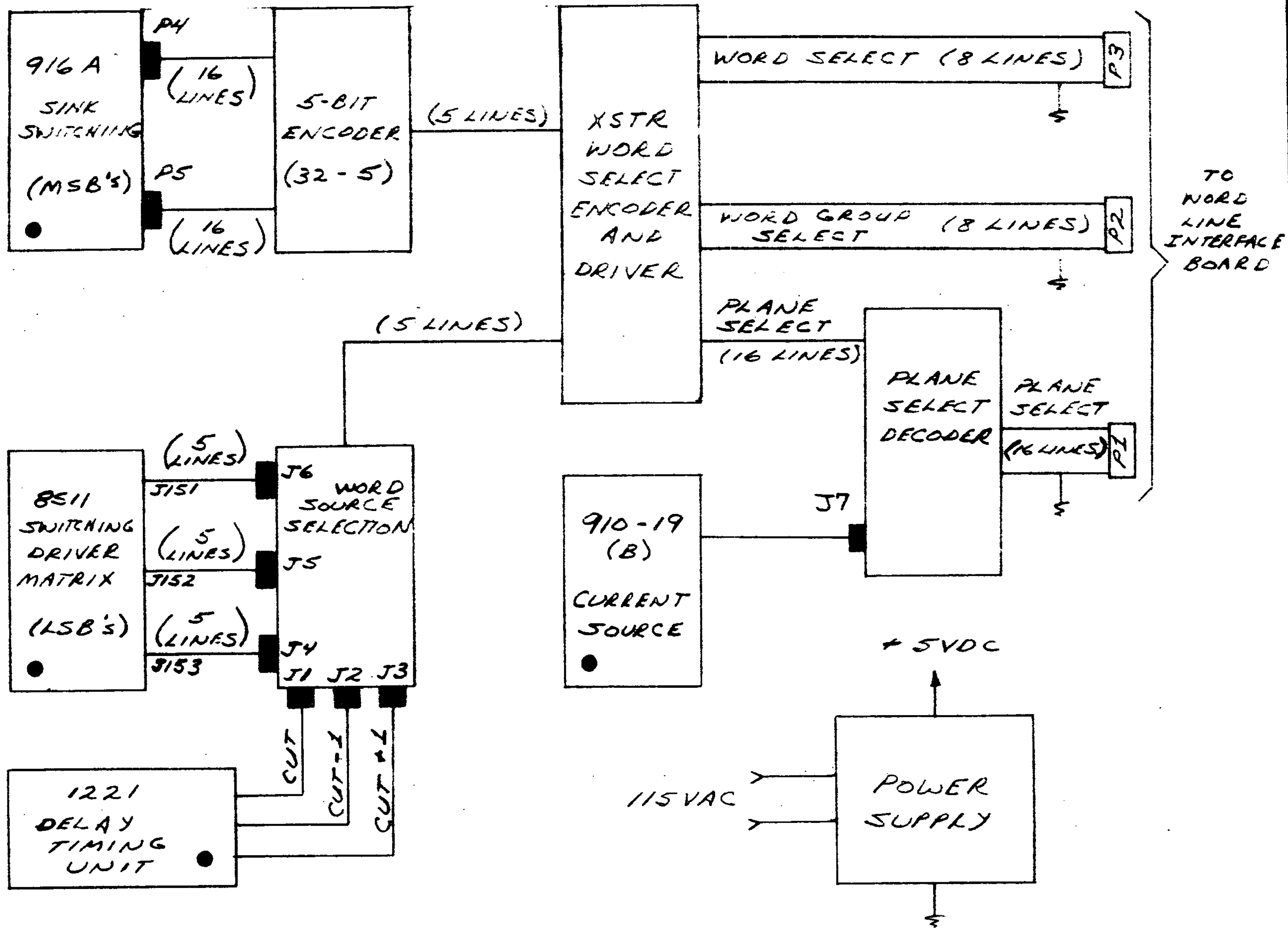
3.4.4.1 Test all outputs at 25 $\pm$ 2°C. Peak amplitude of output shall be 5 millivolts minimum.

3.4.4.2 Test all outputs at +95 $\pm$ 2°C. Peak amplitude of all outputs shall be 5 millivolts minimum.

3.4.4.3 Test all outputs at -45 $\pm$ 2°C. Peak amplitude of all outputs shall be 5 millivolts minimum.

3.4.5 Test Pattern

The test pattern shall be as shown in Figure 5.



● PART OF STACK TESTER

Figure 1: WORD DRIVE TEST FIXTURE INTERCONNECT

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252
AV-2-B-199H-100A-3/69 DWG FORMAT

SIZE A | CODE IDENT NO. 94990 | DWG NO. 12-P1005C
SCALE | REVISION | SHEET 6

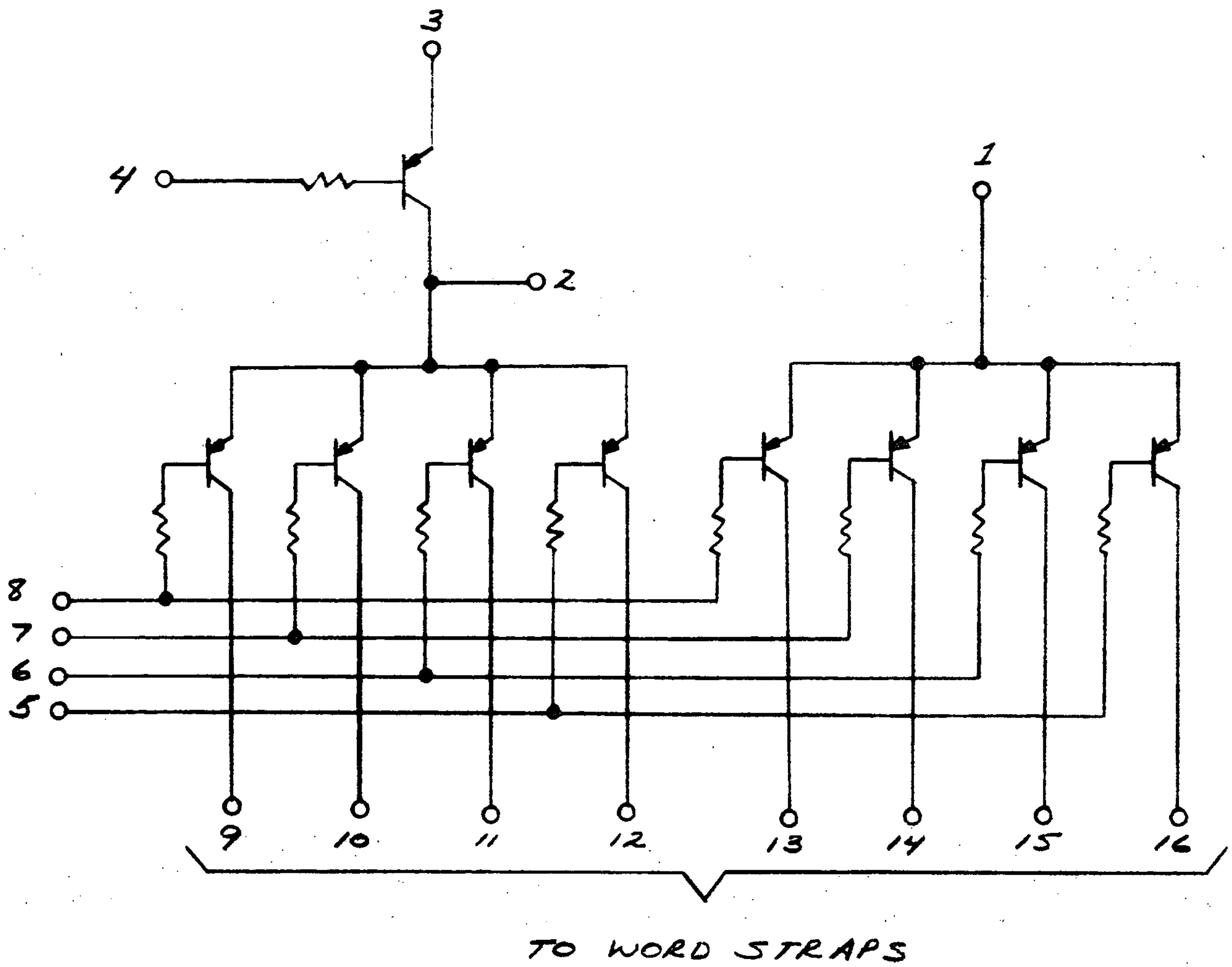
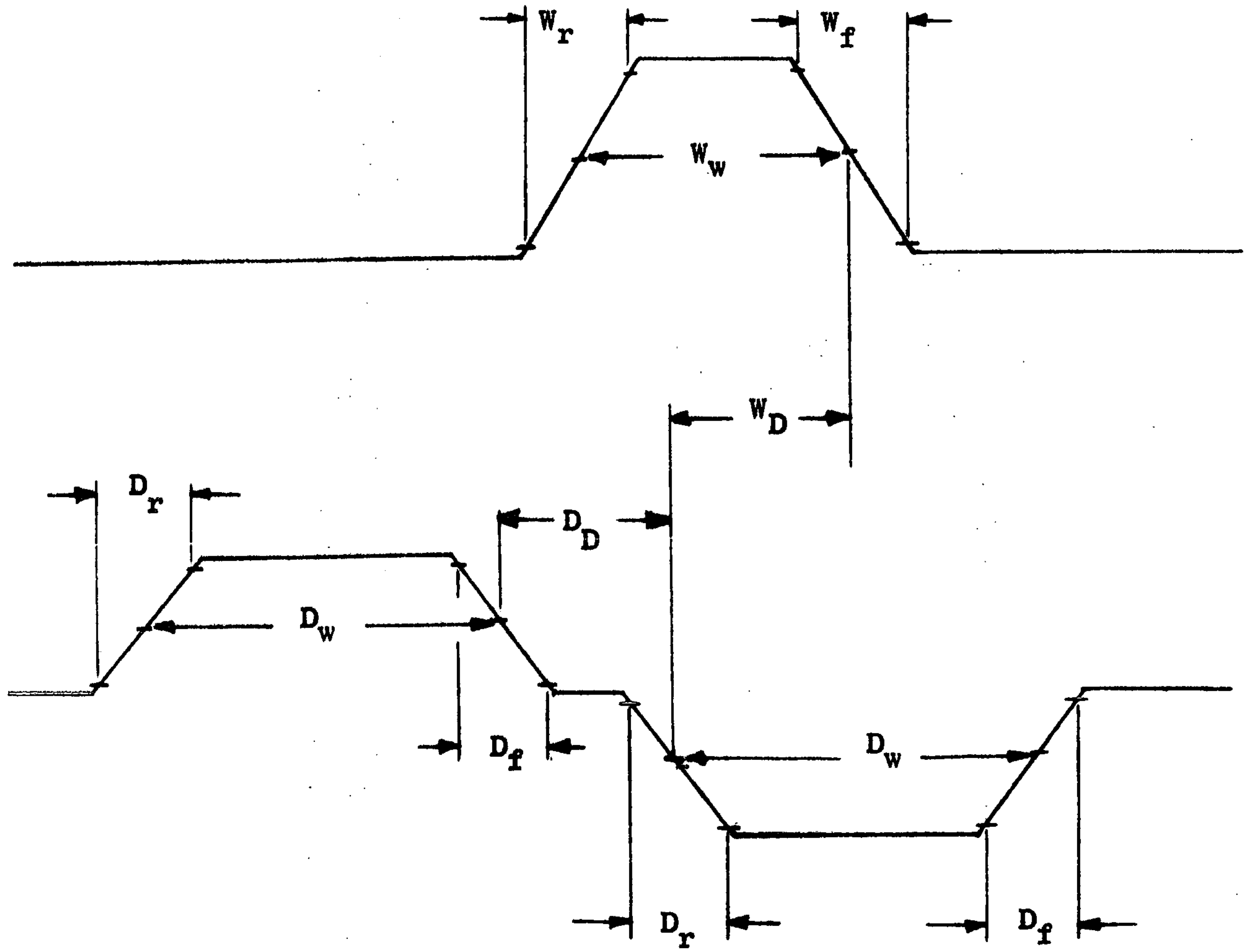


Figure 2: Transistor Switch Matrix

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE A | CODE IDENT NO. 94990 | DWG NO. 12-P11005C
SCALE | REVISION | SHEET 7

AV-2-B-1-99H-100A-3/69 DWG FORMAT



D_r = D_f = 80 ±5 nanoseconds, 10% to 90%

D_W = 220 ±10 nanoseconds, between 50% points.

D_D = 200 ±10 nanoseconds, between 50% points.

W_r = W_f = 90 ±5 nanoseconds, 10% to 90%.

W_W = 200 ±10 nanoseconds, between 50% points.

W_D = 100 ±5 nanoseconds, between 50% points.

FIGURE 3: Current Waveforms

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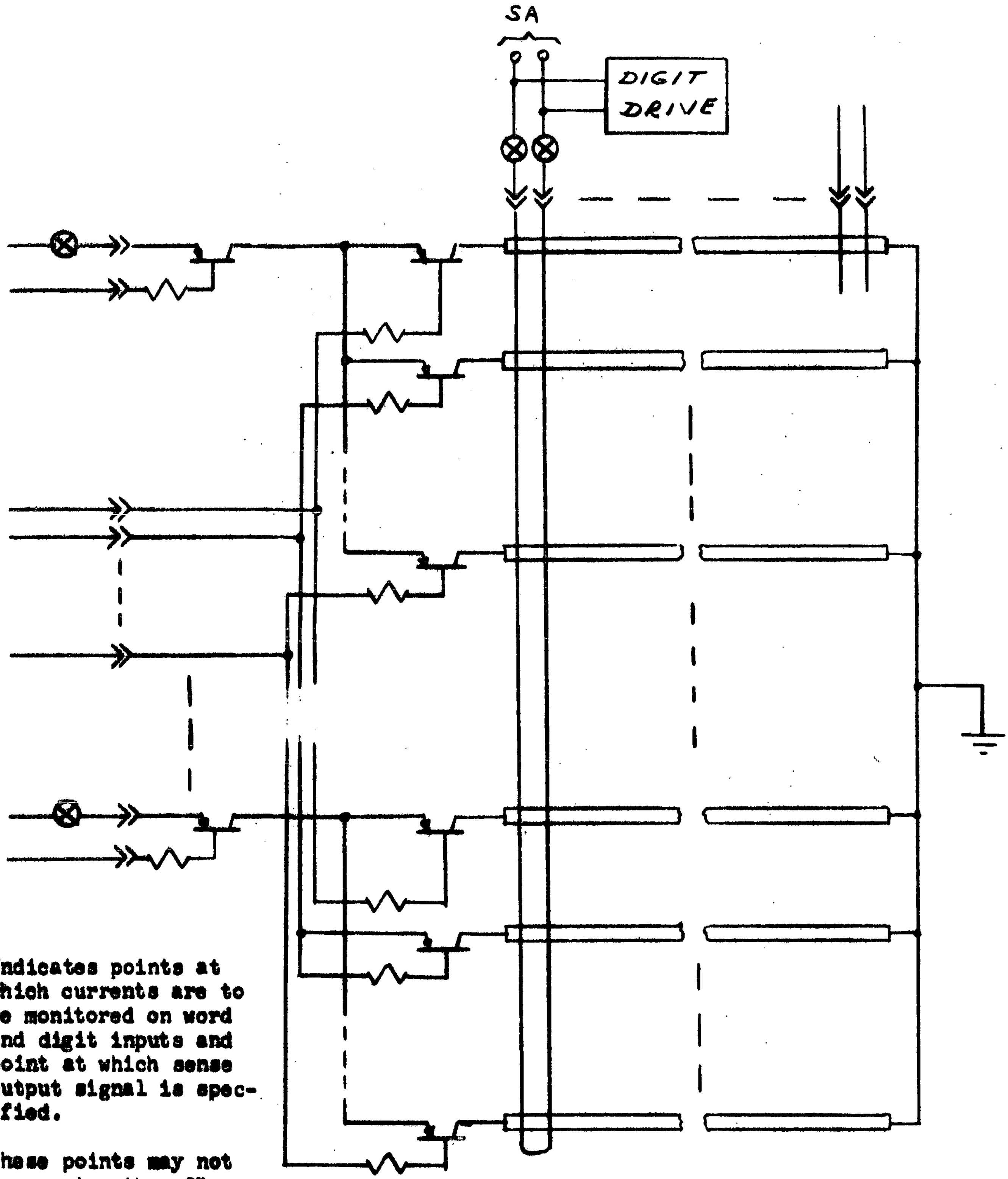
AV-2-B-199H-100A-3/69 DWG FORMAT



Ⓧ Indicates points at which currents are to be monitored on word and digit inputs and point at which sense output signal is specified.

These points may not be greater than 3" from interface connector.

FIGURE 4

Current Monitoring Points

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P11005C
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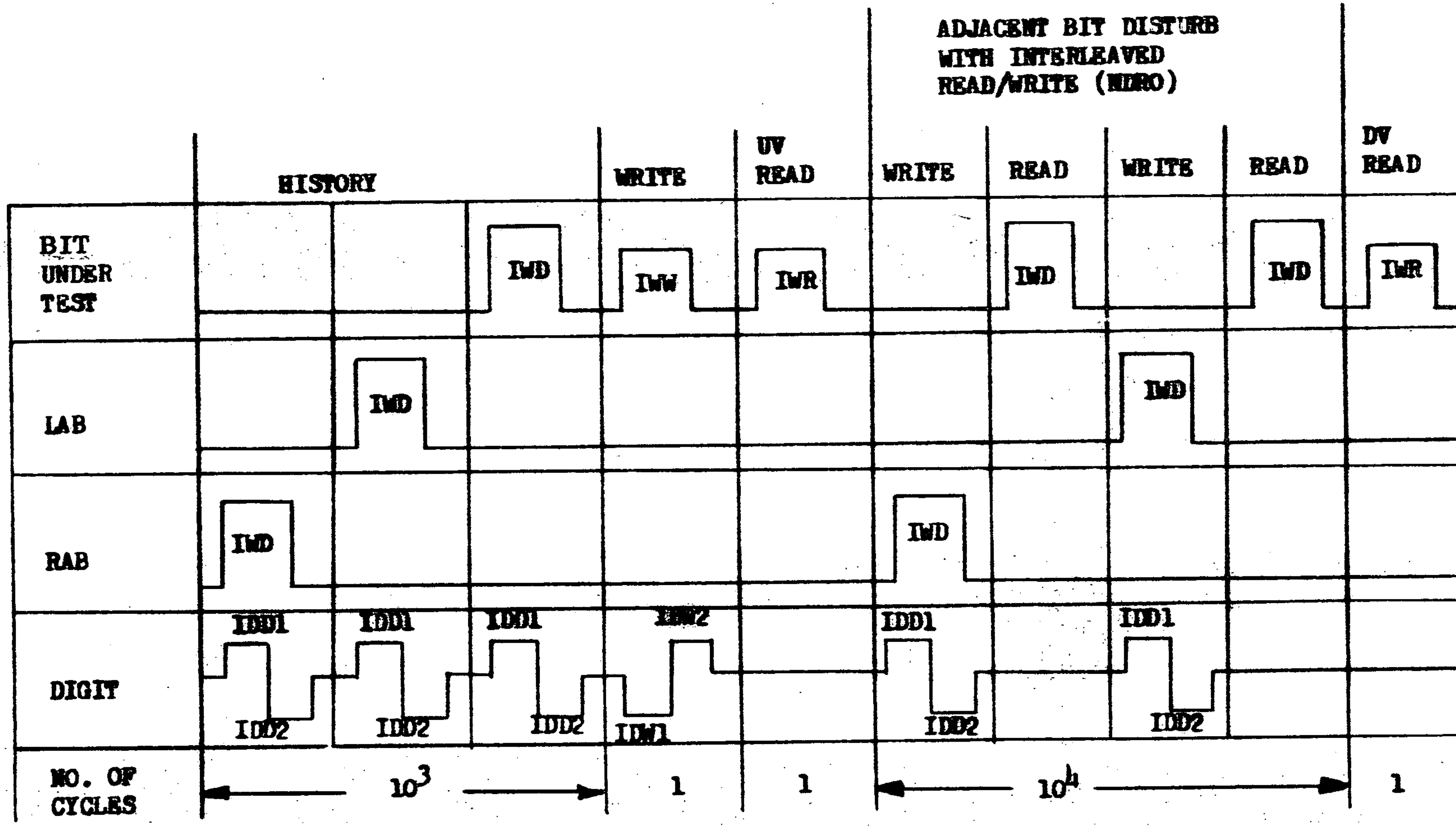
AV-2-B-199H-100A-3/69 DWG FORMAT



ENTIRE PROGRAM REPEATED WITH OPPOSITE POLARITY DIGIT CURRENTS

FIGURE 5: TEST PATTERN

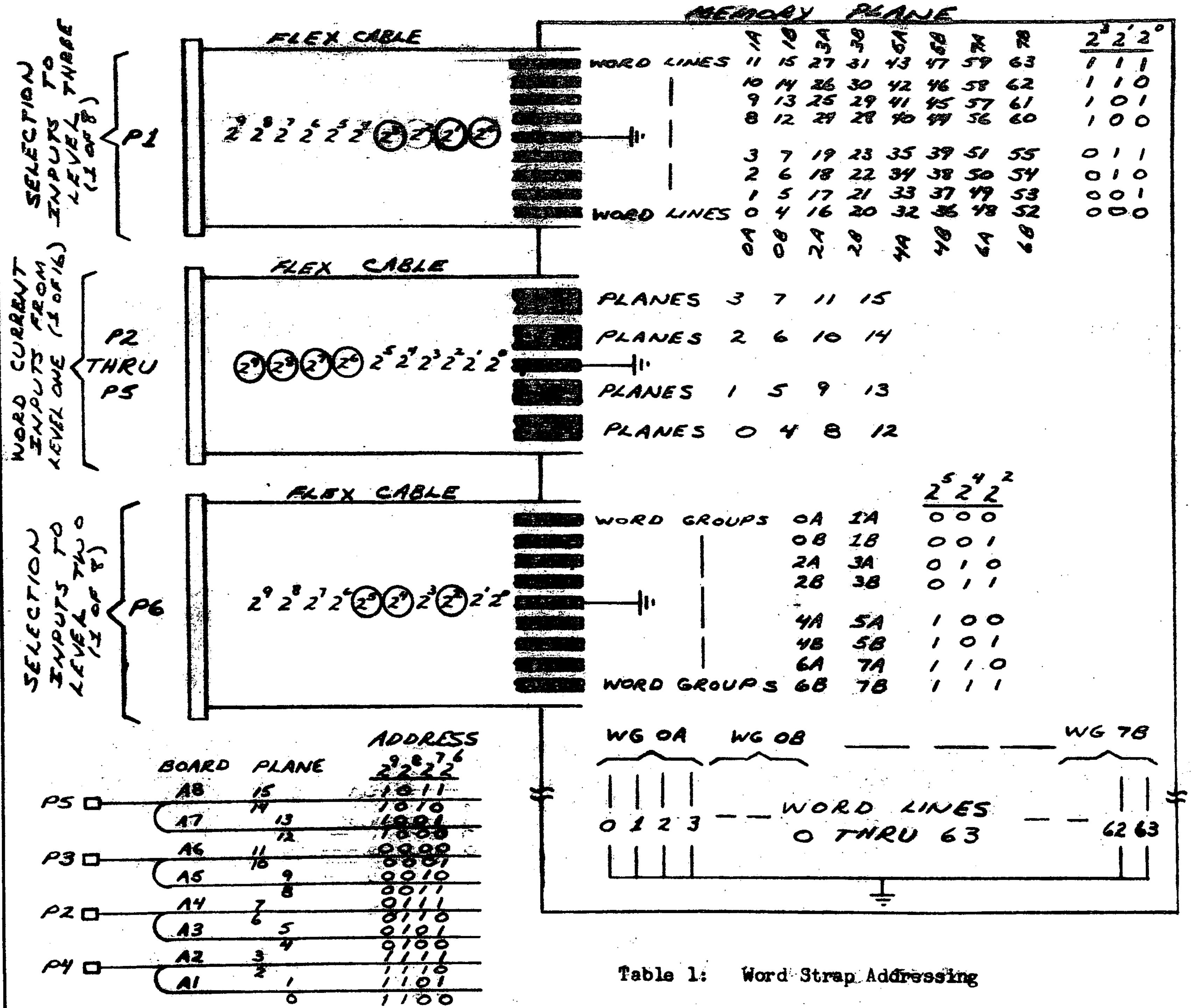


Table 1: Word Strap Addressing

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P11005C

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AV-2-8 1994-1 10-2/69 DWG FORMAT